

ARMY RESEARCH LABORATORY



**Testing of Active Optimized (2nd Pass) Gallium Arsenide
(GaAs) Integrated Circuit Radio Frequency (RF) Booster
Designs for 425 MHz and Dual Band (425 and 900 MHz) in
QFN Packages**

by John E. Penn

ARL-TR-5459

February 2011

NOTICES

Disclaimers

The findings in this report are not to be construed as an official Department of the Army position unless so designated by other authorized documents.

Citation of manufacturer's or trade names does not constitute an official endorsement or approval of the use thereof.

Destroy this report when it is no longer needed. Do not return it to the originator.

Army Research Laboratory

Adelphi, MD 20783-1197

ARL-TR-5459

February 2011

Testing of Active Optimized (2nd Pass) Gallium Arsenide (GaAs) Integrated Circuit Radio Frequency (RF) Booster Designs for 425 MHz and Dual Band (425 and 900 MHz) in QFN Packages

**John E. Penn
Sensors and Electron Devices Directorate, ARL**

REPORT DOCUMENTATION PAGE

*Form Approved
OMB No. 0704-0188*

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing the burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.

PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.

1. REPORT DATE (DD-MM-YYYY)	2. REPORT TYPE		3. DATES COVERED (From - To)	
February 2011				
4. TITLE AND SUBTITLE			5a. CONTRACT NUMBER	
Testing of Active Optimized (2 nd Pass) Gallium Arsenide (GaAs) Integrated Circuit Radio Frequency (RF) Booster Designs for 425 MHz and Dual Band (425 and 900 MHz) in QFN Packages			5b. GRANT NUMBER	
			5c. PROGRAM ELEMENT NUMBER	
			5d. PROJECT NUMBER	
			5e. TASK NUMBER	
			5f. WORK UNIT NUMBER	
6. AUTHOR(S) John E. Penn			8. PERFORMING ORGANIZATION REPORT NUMBER ARL-TR-5459	
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) U.S. Army Research Laboratory ATTN: RDRL-SER-E 2800 Powder Mill Road Adelphi, MD 20783-1197			10. SPONSOR/MONITOR'S ACRONYM(S)	
			11. SPONSOR/MONITOR'S REPORT NUMBER(S)	
12. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release; distribution unlimited.				
13. SUPPLEMENTARY NOTES				
14. ABSTRACT High-performance microwave and radio frequency integrated circuits are of interest to the Army. Several monolithic microwave integrated circuits (MMICs) were designed to enhance the performance of commercial-off-the-shelf (COTS) RF integrated circuits (RFICs) used in many wireless systems. Ten designs in a multi-project prototype GaAs fabrication included active RF front end designs as well as integrated passive matching circuits to reduce SWAP at the system level. The five active MMIC designs were assembled in small QFN packages and tested on PC boards with RF connectors. Small signal and performance measurements were completed for the designs. A previous report documents similar measurements made on the bare MMIC die with an RF probe station.				
15. SUBJECT TERMS MMIC, RFIC, IC, wireless communications				
16. SECURITY CLASSIFICATION OF:		17. LIMITATION OF ABSTRACT UU	18. NUMBER OF PAGES 64	19a. NAME OF RESPONSIBLE PERSON John E. Penn
a. REPORT Unclassified	b. ABSTRACT Unclassified			c. THIS PAGE Unclassified

Contents

List of Figures	iv
List of Tables	v
1. Introduction	1
2. Packaging of 2nd Pass Designs	1
3. Test Results of Packaged 2nd Pass Designs	6
4. Summary of Active Booster IC Designs	51
5. Conclusions	52
6. References	53
List of Symbols, Abbreviations, and Acronyms	54
Distribution List	55

List of Figures

Figure 1. ARL21-ARL24 wire bond diagram in a 4x4mm QFN package.	2
Figure 2. ARL21M425 assembled in a 4x4mm QFN package.	3
Figure 3. ARL22M425 assembled in a 4x4mm QFN package.	4
Figure 4. ARL23M425 assembled in a 4x4mm QFN package.	4
Figure 5. ARL24DB assembled in a 4x4mm QFN package.	5
Figure 6. ARL25 assembled in a 4x4mm QFN package.	5
Figure 7. Example of QFN package and PC board on test block with SMA connectors.	6
Figure 8. Plot of ARL25 test chip (50 & 100 mW PAs, LNA, & TRS).	7
Figure 9. 100 mW PA in package (solid) vs. die (dotted) 2.8 V.	7
Figure 10. 50 mW PA in package (solid) vs. die (dotted) 2.8 V.	8
Figure 11. NB LNA in package (solid) vs. die (dotted) 2.8 V.	8
Figure 12. 100 mW PA power performance at 425 MHz (2.8/3.6 V).	10
Figure 13. 100 mW PA power performance at 450 MHz (2.8/3.6V)	12
Figure 14. 100 mW PA power performance at 500 MHz (2.8/3.6 V).	13
Figure 15. 50 mW PA power performance at 425 MHz (2.8/3.6 V).	15
Figure 16. 50 mW PA power performance at 500 MHz (2.8/3.6 V).	17
Figure 17. Plot of ARL21M425 test chip (BPSK, 100 mW PA, LNA, & TRS).	18
Figure 18. Transmit gain/isolation S21 in package (ARL21M425 at 2.8 V).	19
Figure 19. Relative BPSK transmit phase S21 in package (ARL21M425 at 2.8/3.6 V).	19
Figure 20. Transmit input return loss S11 in package (ARL21M425 at 2.8 V).	20
Figure 21. Transmit output return loss S22 in package (ARL21M425 at 2.8 V).	20
Figure 22. Transmit gain/isolation S21 in package (ARL21M425 at 2.8 V).	21
Figure 23. Receive output return loss in package (ARL21M425 at 2.8 V).	21
Figure 24. Receive input return loss in package (ARL21M425 at 2.8 V).	22
Figure 25. ARL21M425 power performance at 425 MHz (2.8/3.6 V).	24
Figure 26. ARL21M425 power performance at 500 MHz (2.8/3.6 V).	25
Figure 27. Plot of ARL22M425 test chip (BPSK, 50 mW PA, LNA, & TRS).	26
Figure 28. Transmit gain/isolation S21 in package (ARL22M425 at 2.8 V).	27
Figure 29. Relative BPSK transmit phase S21 in package (ARL22M425 at 2.8/3.6 V).	27
Figure 30. Transmit input return loss S11 in package (ARL22M425 at 2.8 V).	28
Figure 31. Transmit output return loss S22 in package (ARL22M425 at 2.8 V).	28

Figure 32. Transmit gain/isolation S21 in package (ARL22M425 at 2.8 V).	29
Figure 33. Receive input return loss in package (ARL22M425 at 2.8 V).	29
Figure 34. Receive output return loss in package (ARL22M425 at 2.8 V).	30
Figure 35. ARL22M425 power performance at 425 MHz (2.8/3.6 V).....	32
Figure 36. ARL22M425 power performance at 500 MHz (2.8/3.6 V).....	33
Figure 37. ARL22M425 power performance at 600 MHz (2.8/3.6 V).....	35
Figure 38. Plot of ARL23M425 test chip (BPSK, broadband PA, broadband LNA, & TRS). ...	36
Figure 39. Transmit gain/isolation S21 in package (ARL23M425 at 2.8 V).	37
Figure 40. Relative BPSK transmit phase S21 in package (ARL23M425 at 2.8/3.6 V).	37
Figure 41. Transmit input return loss S11 in package (ARL23M425 at 2.8 V).	38
Figure 42. Transmit output return loss S22 in package (ARL23M425 at 2.8 V).	38
Figure 43. Transmit gain/isolation S21 in package (ARL23M425 at 2.8 V).	39
Figure 44. Receive input return loss in package (ARL23M425 at 2.8 V).	39
Figure 45. Receive output return loss in package (ARL23M425 at 2.8 V).	40
Figure 46. ARL23M425 power performance at 425 MHz (2.8/3.6 V).....	42
Figure 47. Plot of ARL24DB test chip (broadband BPSK, PA, LNA, & TRS).	43
Figure 48. Transmit gain/isolation S21 in package (ARL24DB at 2.8 V).	44
Figure 49. Relative BPSK transmit phase S21 in package (ARL24DB at 2.8/3.6 V).	44
Figure 50. Transmit input return loss S11 in package (2.8 V).....	45
Figure 51. Transmit output return loss S22 in package (ARL24DB at 2.8 V).	45
Figure 52. Transmit gain/isolation S21 in package (ARL24DB at 2.8 V).	46
Figure 53. Receive input return loss in package (ARL24DB at 2.8 V).	46
Figure 54. Receive output return loss in package (ARL24DB at 2.8 V).	47
Figure 55. ARL24DB power performance at 425 MHz (2.8/3.6 V).....	49
Figure 56. ARL24DB power performance at 900 MHz (2.8/3.6 V).....	50

List of Tables

Table 1. 100 mW PA power performance at 425 MHz (2.8 V).....	9
Table 2. 100 mW PA power performance at 425 MHz (3.6 V).....	10
Table 3. 100 mW PA power performance at 450 MHz (2.8 V).....	11
Table 4. 100 mW PA power performance at 450 MHz (3.6 V).....	11
Table 5. 100 mW PA power performance at 500 MHz (2.8 V).....	12

Table 6. 100 mW PA power performance at 500 MHz (3.6 V).....	13
Table 7. 50 mW PA power performance at 425 MHz (2.8 V).....	14
Table 8. 50 mW PA power performance at 425 MHz (3.6 V).....	15
Table 9. 50 mW PA power performance at 500 MHz (2.8 V).....	16
Table 10. 50 mW PA power performance at 500 MHz (3.6 V).....	16
Table 11. LNA noise figure performance at 2.8 V and 3 mA DC bias.	17
Table 12. ARL21M425 power performance at 425 MHz (2.8 V).....	23
Table 13. ARL21M425 power performance at 425 MHz (3.6 V).....	23
Table 14. ARL21M425 power performance at 500 MHz (2.8 V).....	24
Table 15. ARL21M425 power performance at 500 MHz (3.6 V).....	25
Table 16. ARL22M425 power performance at 425 MHz (2.8 V).....	31
Table 17. ARL22M425 power performance at 425 MHz (3.6 V).....	31
Table 18. ARL22M425 power performance at 500 MHz (2.8 V).....	32
Table 19. ARL22M425 power performance at 500 MHz (3.6 V).....	33
Table 20. ARL22M425 power performance at 600 MHz (2.8 V).....	34
Table 21. ARL22M425 power performance at 600 MHz (3.6 V).....	34
Table 22. ARL23M425 power performance at 425 MHz (2.8 V).....	41
Table 23. ARL23M425 power performance at 425 MHz (3.6 V).....	41
Table 24. ARL24DB power performance at 425 MHz (2.8 V).....	48
Table 25. ARL24DB power performance at 425 MHz (3.6 V).....	48
Table 26. ARL24DB power performance at 900 MHz (2.8 V).....	49
Table 27. ARL24DB power performance at 900 MHz (3.6 V).....	50

1. Introduction

Increased transmission range in low-power radio frequency (RF) applications is a desired commodity within the Army. The RF integrated circuit (RFIC) booster chip is intended to increase range between RF nodes for low-power wireless applications. The booster concept uses the high RF performance advantages of the gallium arsenide (GaAs) process to enhance the capabilities of systems using commercial RFIC transceivers. It can be inserted easily into systems to increase transmit power, receiver sensitivity, and efficient battery use. Probe testing of bare die for the 2nd pass optimized booster designs has been documented previously. The active designs were assembled in quad flat no-lead (QFN) packages and tested on small printed circuit (PC) boards. This documents the performance of the packaged 2nd pass RF Booster ICs.

2. Packaging of 2nd Pass Designs

The focus of the 2nd pass was predominantly for the 400 to 450 MHz frequency band, but there was also a desire to have a broadband or dual band capability below 1 GHz. Matching circuits were included in the 2nd pass GaAs integrated circuit (IC) designs, but are not documented as part of these board level tests. Only the standalone active designs, which are matched to 50 ohm single ended RF connections for the antenna, transmit input, and receive output, were tested for RF performance in QFN packages. Optimal custom monolithic microwave integrated circuit (MMIC) design requires knowledge of the intended packaging of the device to absorb package parasitics at microwave frequencies. Fortunately, the relatively low frequencies, less than 1 GHz, of these designs minimize the impact of the wire bonds used to attach the GaAs ICs within the QFN package.

The 4x4mm QFN packages from the 1st pass designs were re-used to package the 2nd pass designs. Also, spare test boards fabricated for the 1st pass designs were re-used to test the 2nd pass designs, saving considerable schedule time, and expense. ARL Technical Report ARL-TR-5131, “Testing of GaAs Microwave Integrated Circuit Designs in QFN Packages” by John Penn, documents the QFN package level tests performed on the 1st pass Booster IC designs.

There were several design variations in the 2nd pass tile intending to optimize for different design goals. All four active RF front end designs contain a binary phase shift keying (BPSK) modulator, a power amplifier for transmission, a low noise amplifier for reception, and a low loss transmit/receive (TR) switch. Figure 1 shows the typical wire bond diagram for assembly of the active designs in the 4x4mm QFN package. On the left side is the RF input and RF output, presumably close to the commercial off the shelf (COTS) RFIC in a board layout. The right side is the RF antenna connection. On the top side is the VDD supply for the Power Amplifier

(transmit) along with the differential driver inputs for the BPSK modulator. On the bottom side is the VDD supply for the Low Noise Amplifier (receive) and the differential switch inputs for the TR switch.

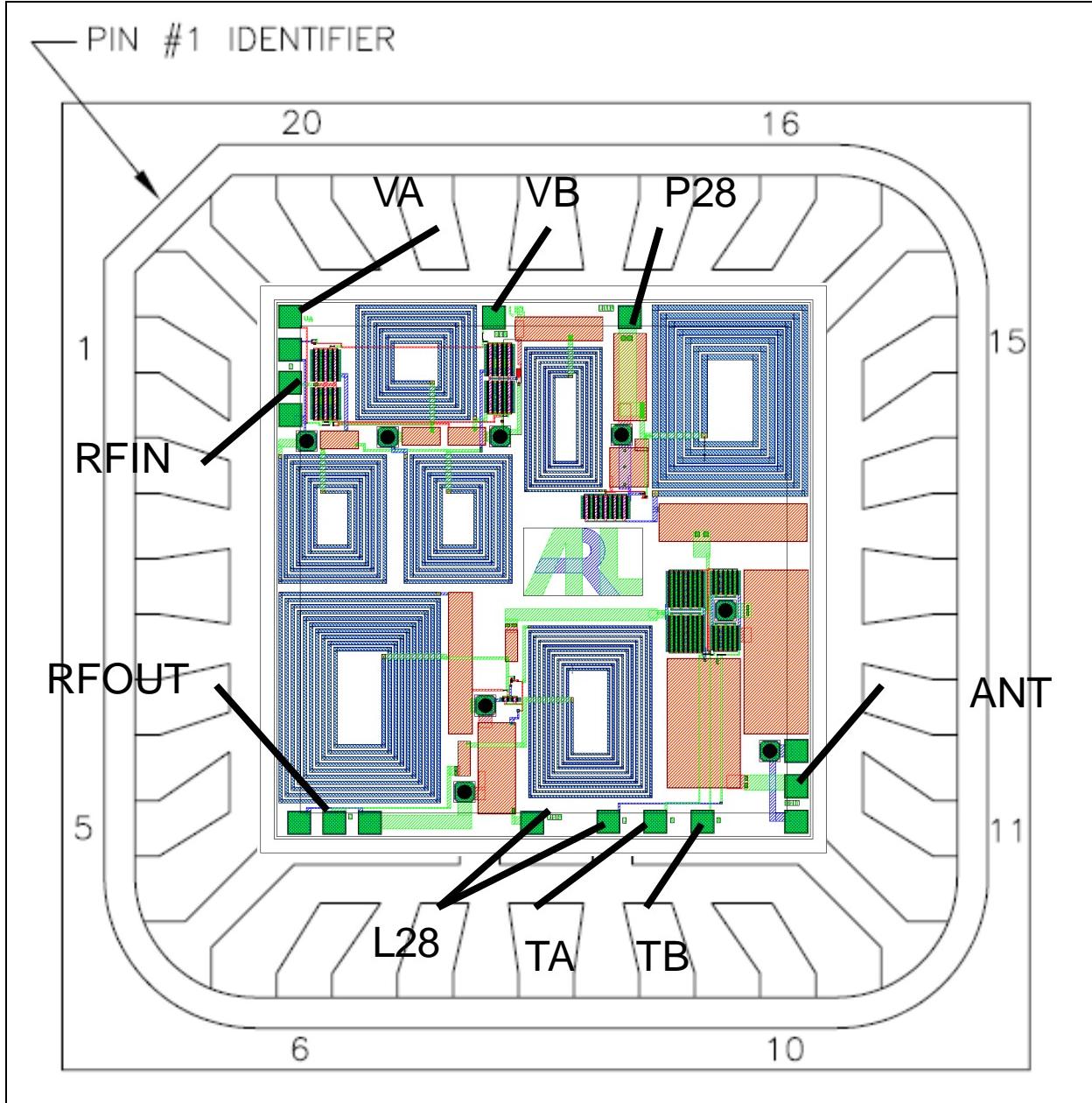


Figure 1. ARL21-ARL24 wire bond diagram in a 4x4mm QFN package.

The first design variation, ARL21M425, is intended for the 400 to 450 MHz UHF band and had a goal of 100 mW of RF output power in a 3 V battery powered system. A second design, ARL22M425, is nearly identical, but replaces the power amplifier with one designed for a goal of 50 mW of RF output power in a 3 V system. The power amplifier from the 1st pass designs was a broadband stable feedback design that worked well in a 3 V or a 3.9 V battery system with

very good efficiency and was used for a third design, ARL23M425. Lastly, the fourth variation, ARL24DB, was intended to be broad band, or at least dual band for the 400 and 900 MHz ultra-high frequency (UHF) bands. ARL24DB used the broadband 1st pass amplifier design, a modified lower current broadband 1st pass low noise amplifier, and a newly designed dual band BPSK modulator. The only portion of the dual band design common with all four designs is the broadband positive control voltage TR switch. Figures 2 through 5, show the first four designs assembled in 4x4mm QFN packages on a test board. A test chip, ARL25, contains separate circuits for the 50 mW power amplifier, 100 mW power amplifier, narrowband low current (3 mA) low noise amplifier, and the TR switch. Figure 6 shows the test chip assembled in a 4x4mm QFN package on a test board for testing the three amplifier circuits. Figure 7 shows a typical test board from the 1st pass designs used to test the QFN packaged Booster ICs using a test block with SMA connectors. After verifying that the packaged IC functions within the test block, SMA connectors are soldered to the board and capacitors are added to the DC supply inputs.

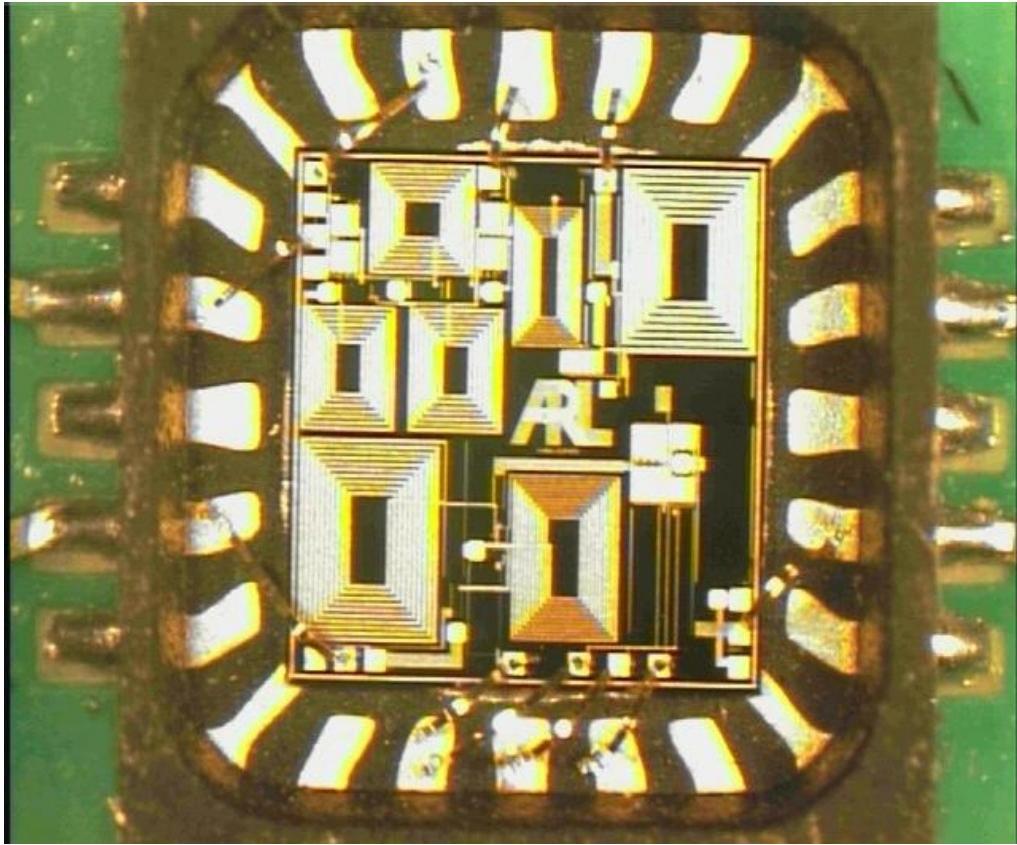


Figure 2. ARL21M425 assembled in a 4x4mm QFN package.

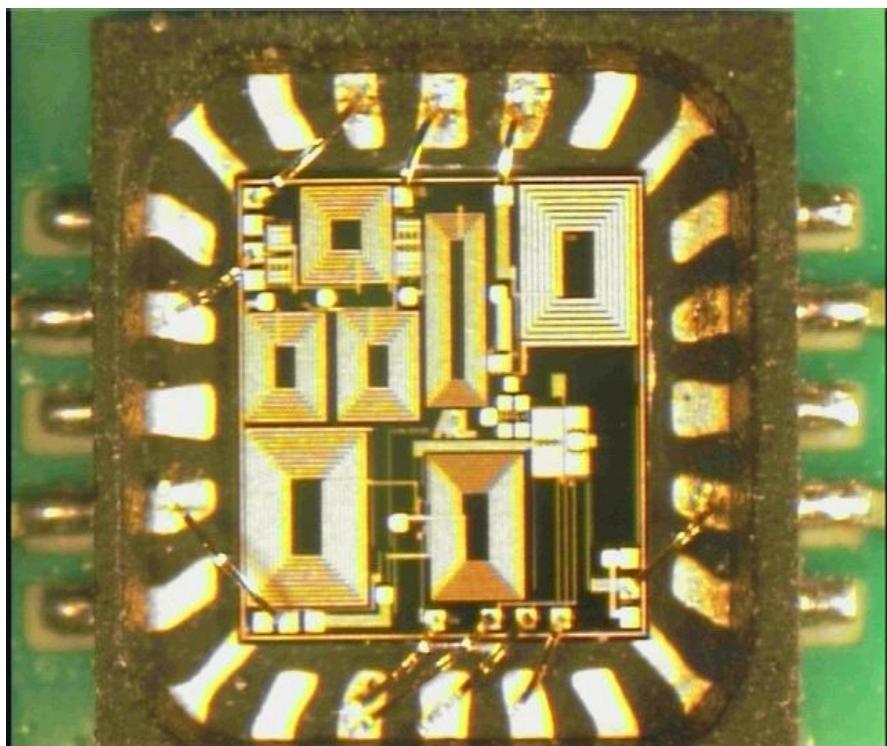


Figure 3. ARL22M425 assembled in a 4x4mm QFN package.

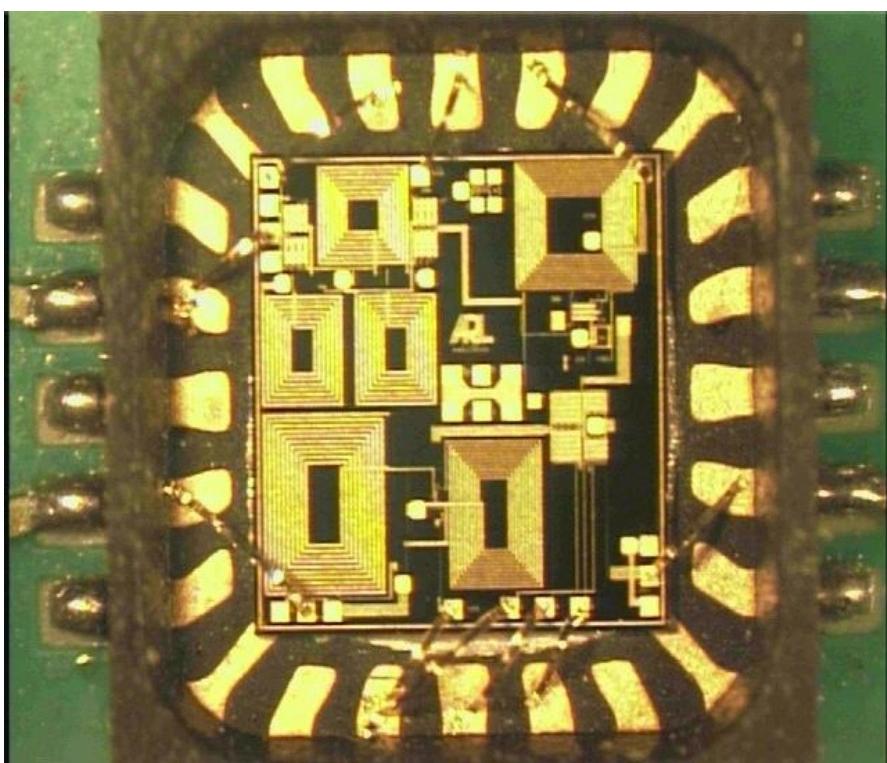


Figure 4. ARL23M425 assembled in a 4x4mm QFN package.

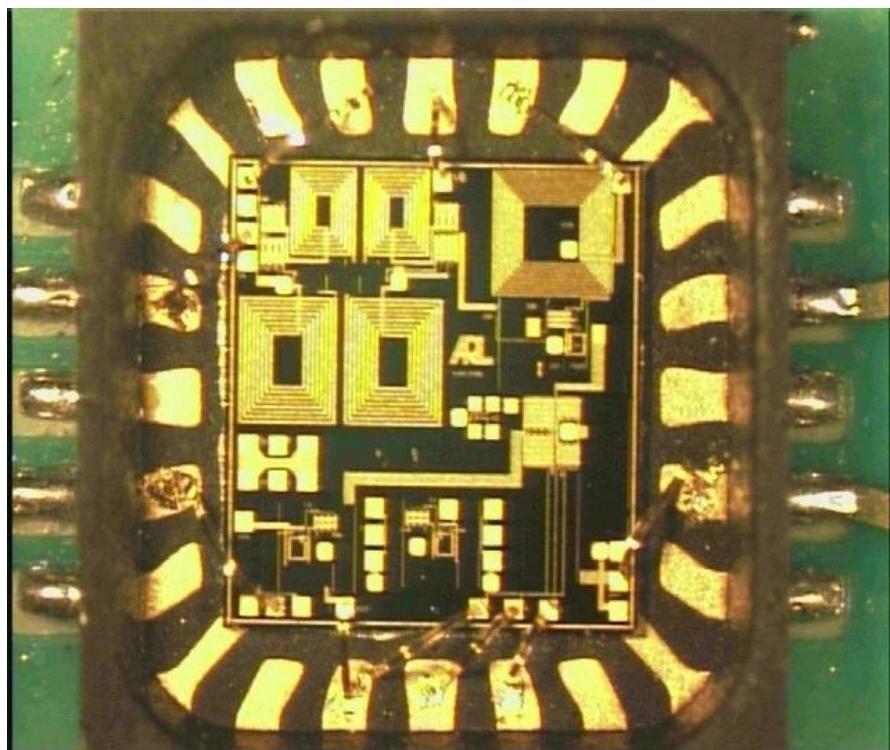


Figure 5. ARL24DB assembled in a 4x4mm QFN package.

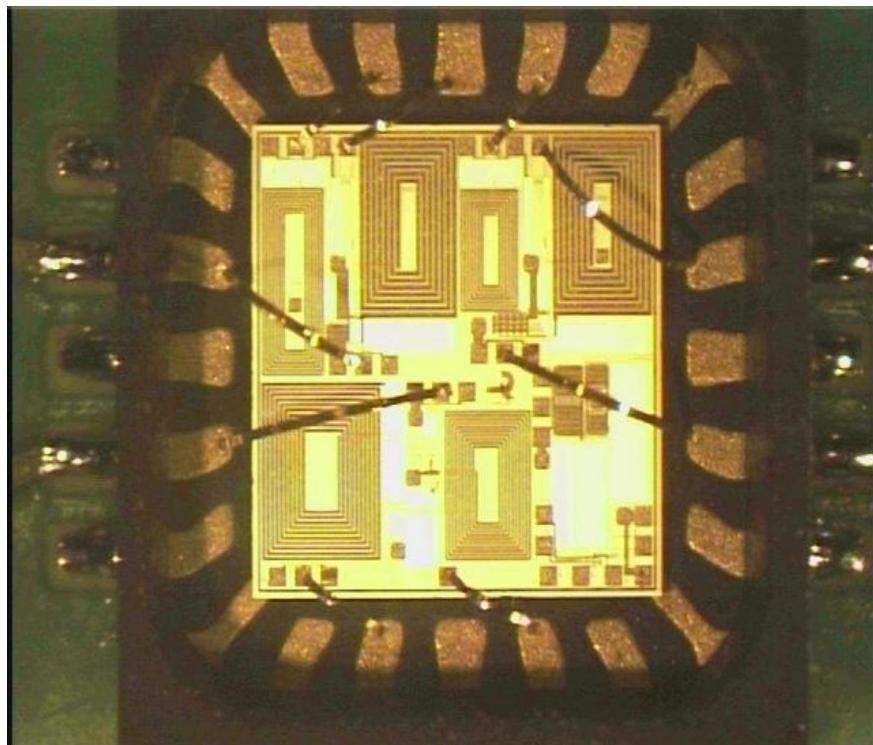


Figure 6. ARL25 assembled in a 4x4mm QFN package.

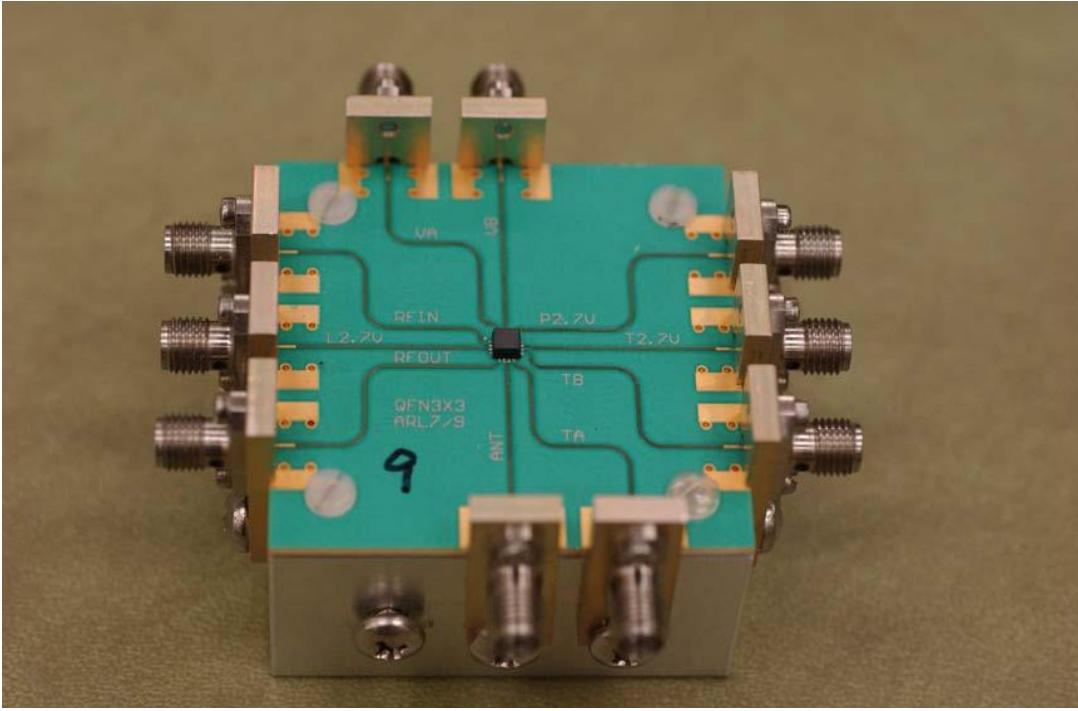


Figure 7. Example of QFN package and PC board on test block with SMA connectors.

3. Test Results of Packaged 2nd Pass Designs

The designs have previously been probe tested so the packaged results are expected to be similar to those measurements with some minor additional parasitic effects from the wire bonds and QFN package. First, the individual amplifiers of the test chip, ARL25 (see plot in figure 8), are shown with s-parameter comparisons between the packaged and probed die measurements. Additional power performance measurements for the transmit/power amplifiers are shown, as well as, gain and noise figure measurements for the receive/low noise amplifiers. Figure 9 shows reasonably good agreement between the bare die and packaged 100 mW power amplifier. Small signal gain was about 21.5 dB at 445 MHz with a DC bias of 2.8 V at 76 mA. Likewise, figure 10 shows the 50 mW power amplifier which had a lower gain of 18.3 dB at 450 MHz for a DC bias of 2.8 V at 38 mA, and also had a poor output return loss compared to the 100 mW power amplifier. The poor output return loss is due to the design compromise match for output power over return loss. Figure 11 shows the low noise amplifier at 2.8 V at 3 mA IDS bias with almost 10 dB of gain at 440 MHz and similar performance between the packaged part and the bare die measurements. Performance measurements for the individual amplifiers follow.

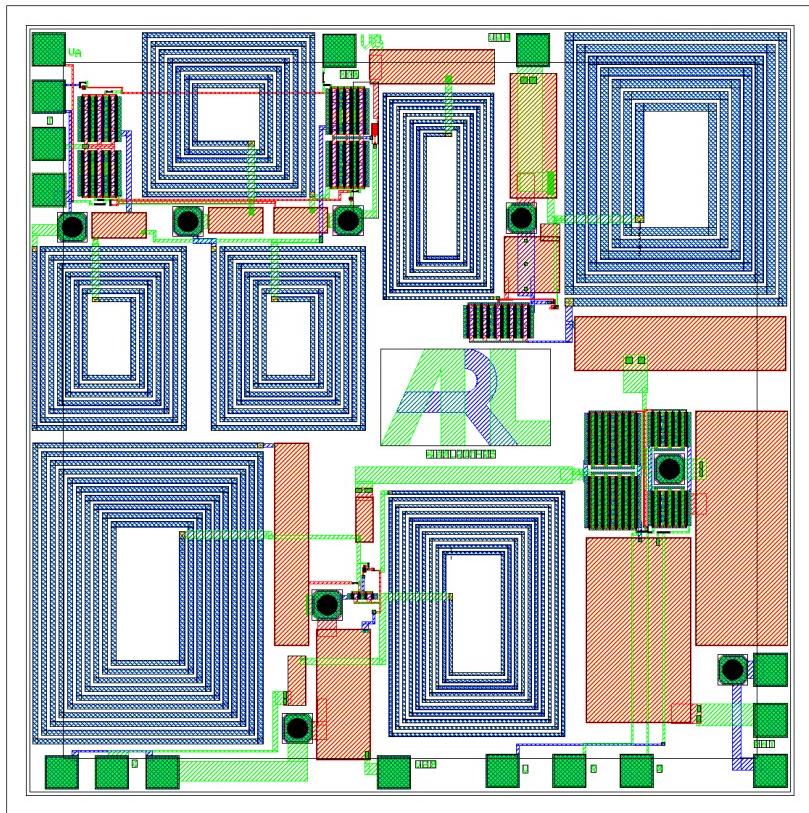


Figure 8. Plot of ARL25 test chip (50 & 100 mW PAs, LNA, & TRS).

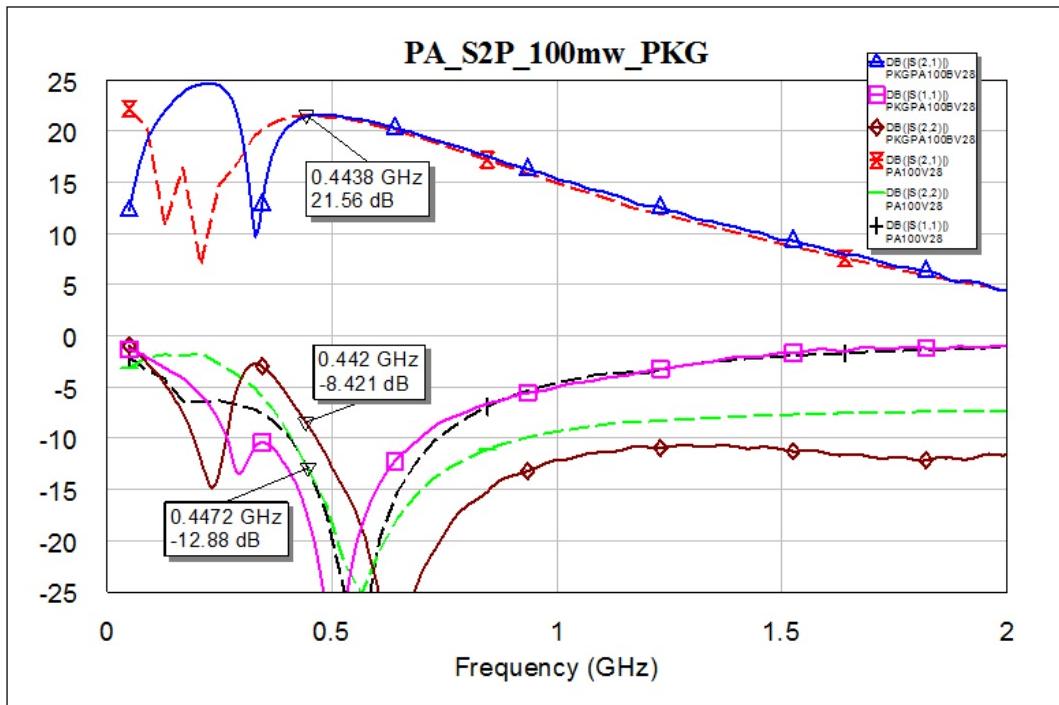


Figure 9. 100 mW PA in package (solid) vs. die (dotted) 2.8 V.

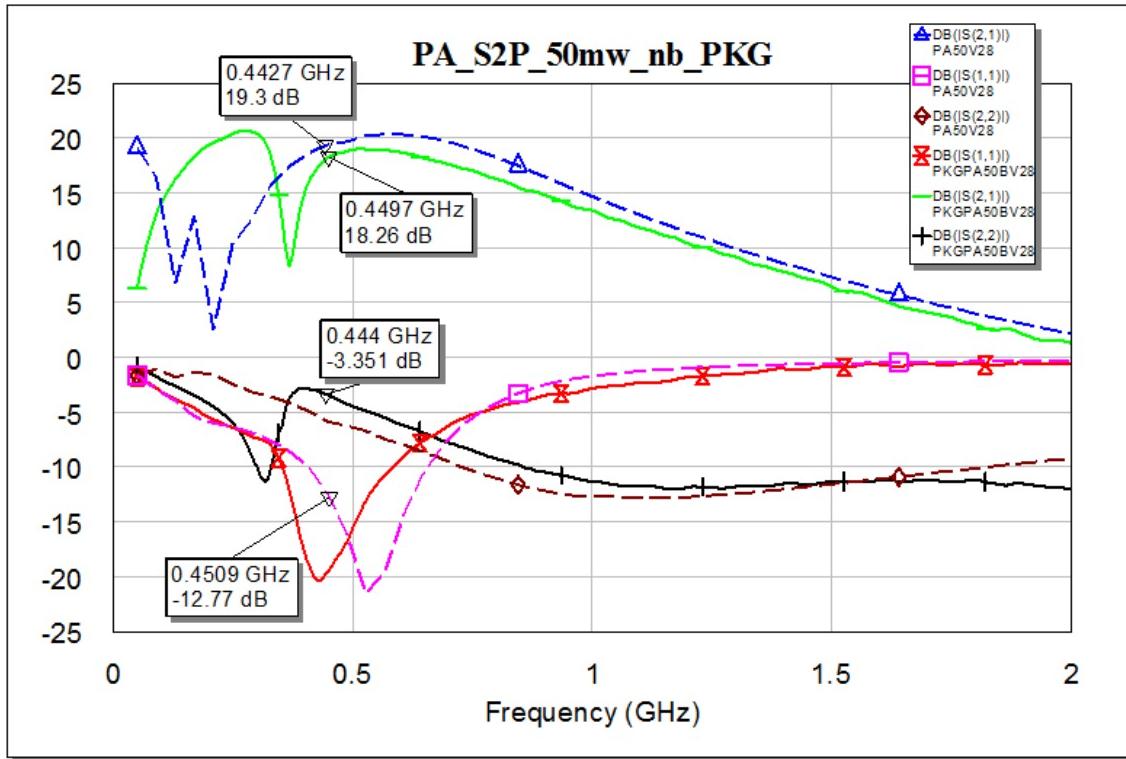


Figure 10. 50 mW PA in package (solid) vs. die (dotted) 2.8 V.

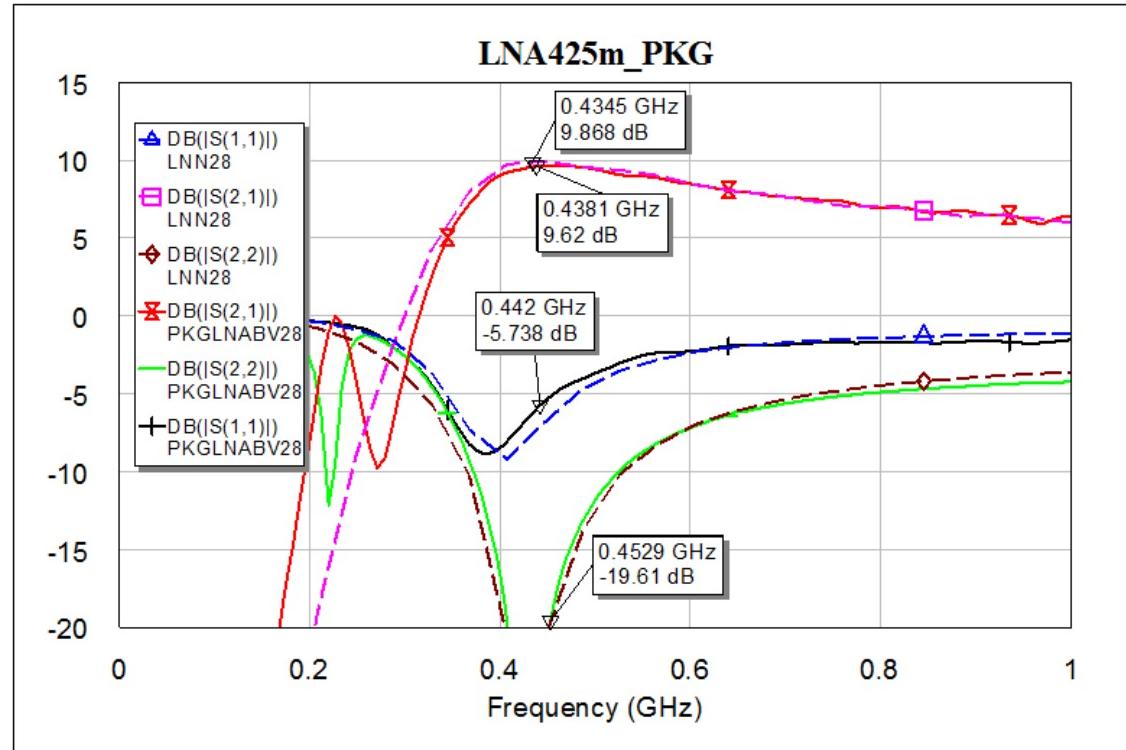


Figure 11. NB LNA in package (solid) vs. die (dotted) 2.8 V.

100 mW Power Amplifier: I measured the RF output power of the packaged amplifier versus the input power to yield power added efficiency, gain, and DC power consumption. These measurements were performed at 2.8 V and 3.6 V, presuming a regulated power supply from either a 3.0 V battery or a 3.9 V lithium battery, at 425 MHz, 450 MHz, and 500 MHz. Table 1 shows the measured performance at 2.8 V and 425 MHz, while table 2 is at 3.6 V. Figure 12, shows a plot summarizing the measurements versus RF input power. Tables 3 and 4, plus figure 13, show the performance at 450 MHz which is somewhat improved over the 425 MHz measurements. At 500 MHz, the performance is even better as shown in tables 5 and 6, and summarized by the plot of figure 14. At 3 dB compression, the power added efficiency is good at 38% to 40% and increases a bit at higher compression levels, i.e., higher RF input levels. At 450 MHz and 2.8 V, the 100 mW output power goal is about 1 dB low (80 mW), but is easily achieved at 3.6 V (113 mW). This design had slightly lower gain and less output power than predicted from the original simulations, but some of this could be normal process variation. Also, the Triquint TOM3 model is known to over predict the output power by about 1 dB. A newer version 4 model (TOM4) is supposed to be more accurate, but does not converge well in simulations. Performance of this amplifier within the RF Booster ICs will be slightly less due to the 0.5 dB insertion loss of the TR switch on its output. Overall, this design performed well and would be preferred to the 50 mW variation described next.

Table 1. 100 mW PA power performance at 425 MHz (2.8 V).

12/22/2010 Measured with Power Meter									
425 MHz	Package #1 ARL25 PA100mW ARLTILE2 TQPED					2.8V ; 76 mA			
Pin(SG)	Pout(PM)	Pin(corr)	Pout(corr)	Gain	I1(2.8V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	1.38	-20.20	1.38	21.58	76	212.8	1.37	0.6	0.6
-15.0	6.33	-15.20	6.33	21.53	76	212.8	4.30	2.0	2.0
-10.0	11.25	-10.20	11.25	21.45	75	210.0	13.34	6.4	6.3
-8.0	13.21	-8.20	13.21	21.41	75	210.0	20.94	10.0	9.9
-6.0	15.07	-6.20	15.07	21.27	75	210.0	32.14	15.3	15.2
-4.0	16.68	-4.20	16.68	20.88	76	212.8	46.56	21.9	21.7
-3.0	17.30	-3.20	17.30	20.50	77	215.6	53.70	24.9	24.7
-2.0	17.80	-2.20	17.80	20.00	77	215.6	60.26	27.9	27.7
-1.0	18.20	-1.20	18.20	19.40	78	218.4	66.07	30.3	29.9
0.0	18.53	-0.20	18.53	18.73	78	218.4	71.29	32.6	32.2
1.0	18.78	0.80	18.78	17.98	77	215.6	75.51	35.0	34.5
2.0	18.96	1.80	18.96	17.16	76	212.8	78.70	37.0	36.3

Table 2. 100 mW PA power performance at 425 MHz (3.6 V).

12/22/2010	Measured with Power Meter									
425 MHz	Package # ARL25 PA100mW ARLTILE2 TQPED					3.6V ; 79 mA				
Pin(SG)	Pout(PM)	Pin(corr)	Pout(corr)	Gain	I1(3.6V)	PDC(mw)	Pout(mw)	Drn Eff	PAE	
-20.0	1.34	-20.20	1.34	21.54	79	284.4	1.36	0.5	0.5	
-15.0	6.27	-15.20	6.27	21.47	79	284.4	4.24	1.5	1.5	
-10.0	11.11	-10.20	11.11	21.31	79	284.4	12.91	4.5	4.5	
-8.0	13.06	-8.20	13.06	21.26	79	284.4	20.23	7.1	7.1	
-6.0	14.96	-6.20	14.96	21.16	79	284.4	31.33	11.0	10.9	
-4.0	16.75	-4.20	16.75	20.95	80	288.0	47.32	16.4	16.3	
-3.0	17.57	-3.20	17.57	20.77	81	291.6	57.15	19.6	19.4	
-2.0	18.30	-2.20	18.30	20.50	83	298.8	67.61	22.6	22.4	
-1.0	18.92	-1.20	18.92	20.12	85	306.0	77.98	25.5	25.2	
0.0	19.45	-0.20	19.45	19.65	86	309.6	88.10	28.5	28.1	
1.0	19.86	0.80	19.86	19.06	87	313.2	96.83	30.9	30.5	
2.0	20.16	1.80	20.16	18.36	86	309.6	103.75	33.5	33.0	
3.0	20.38	2.80	20.38	17.58	85	306.0	109.14	35.7	35.0	

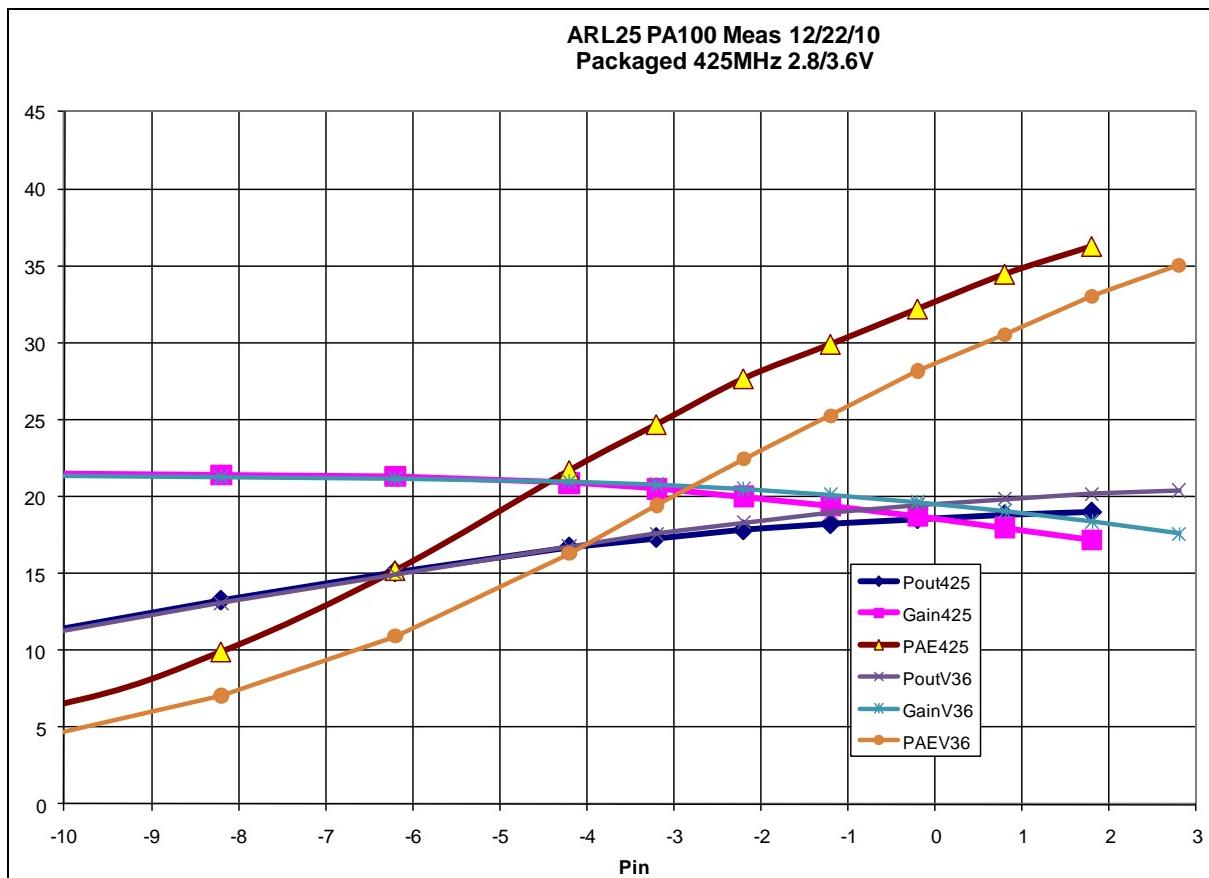


Figure 12. 100 mW PA power performance at 425 MHz (2.8/3.6 V).

Table 3. 100 mW PA power performance at 450 MHz (2.8 V).

12/22/2010 Measured with Power Meter		450 MHz Package #1 ARL25 PA100mW ARLTILE2 TQPED					2.8V ; 76 mA		
Pin(SG)	Pout(PM)	Pin(corr)	Pout(corr)	Gain	I1(2.8V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	1.77	-20.20	1.77	21.97	76	212.8	1.50	0.7	0.7
-15.0	6.73	-15.20	6.73	21.93	76	212.8	4.71	2.2	2.2
-10.0	11.67	-10.20	11.67	21.87	75	210.0	14.69	7.0	6.9
-8.0	13.73	-8.20	13.73	21.93	74	207.2	23.60	11.4	11.3
-6.0	15.57	-6.20	15.57	21.77	74	207.2	36.06	17.4	17.3
-4.0	17.09	-4.20	17.09	21.29	73	204.4	51.17	25.0	24.8
-3.0	17.68	-3.20	17.68	20.88	73	204.4	58.61	28.7	28.4
-2.0	18.15	-2.20	18.15	20.35	72	201.6	65.31	32.4	32.1
-1.0	18.52	-1.20	18.52	19.72	72	201.6	71.12	35.3	34.9
0.0	18.81	-0.20	18.81	19.01	72	201.6	76.03	37.7	37.2
1.0	19.04	0.80	19.04	18.24	72	201.6	80.17	39.8	39.2
2.0	19.22	1.80	19.22	17.42	71	198.8	83.56	42.0	41.3

Table 4. 100 mW PA power performance at 450 MHz (3.6 V).

12/22/2010 Measured with Power Meter		450 MHz Package # ARL25 PA100mW ARLTILE2 TQPED					3.6V ; 79 mA		
Pin(SG)	Pout(PM)	Pin(corr)	Pout(corr)	Gain	I1(3.6V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	1.70	-20.20	1.70	21.90	79	284.4	1.48	0.5	0.5
-15.0	6.65	-15.20	6.65	21.85	79	284.4	4.62	1.6	1.6
-10.0	11.58	-10.20	11.58	21.78	78	280.8	14.39	5.1	5.1
-8.0	13.64	-8.20	13.64	21.84	78	280.8	23.12	8.2	8.2
-6.0	15.56	-6.20	15.56	21.76	78	280.8	35.97	12.8	12.7
-4.0	17.39	-4.20	17.39	21.59	78	280.8	54.83	19.5	19.4
-3.0	18.21	-3.20	18.21	21.41	79	284.4	66.22	23.3	23.1
-2.0	18.92	-2.20	18.92	21.12	80	288.0	77.98	27.1	26.9
-1.0	19.48	-1.20	19.48	20.68	82	295.2	88.72	30.1	29.8
0.0	19.92	-0.20	19.92	20.12	83	298.8	98.17	32.9	32.5
1.0	20.26	0.80	20.26	19.46	83	298.8	106.17	35.5	35.1
2.0	20.53	1.80	20.53	18.73	83	298.8	112.98	37.8	37.3
3.0	20.74	2.80	20.74	17.94	82	295.2	118.58	40.2	39.5

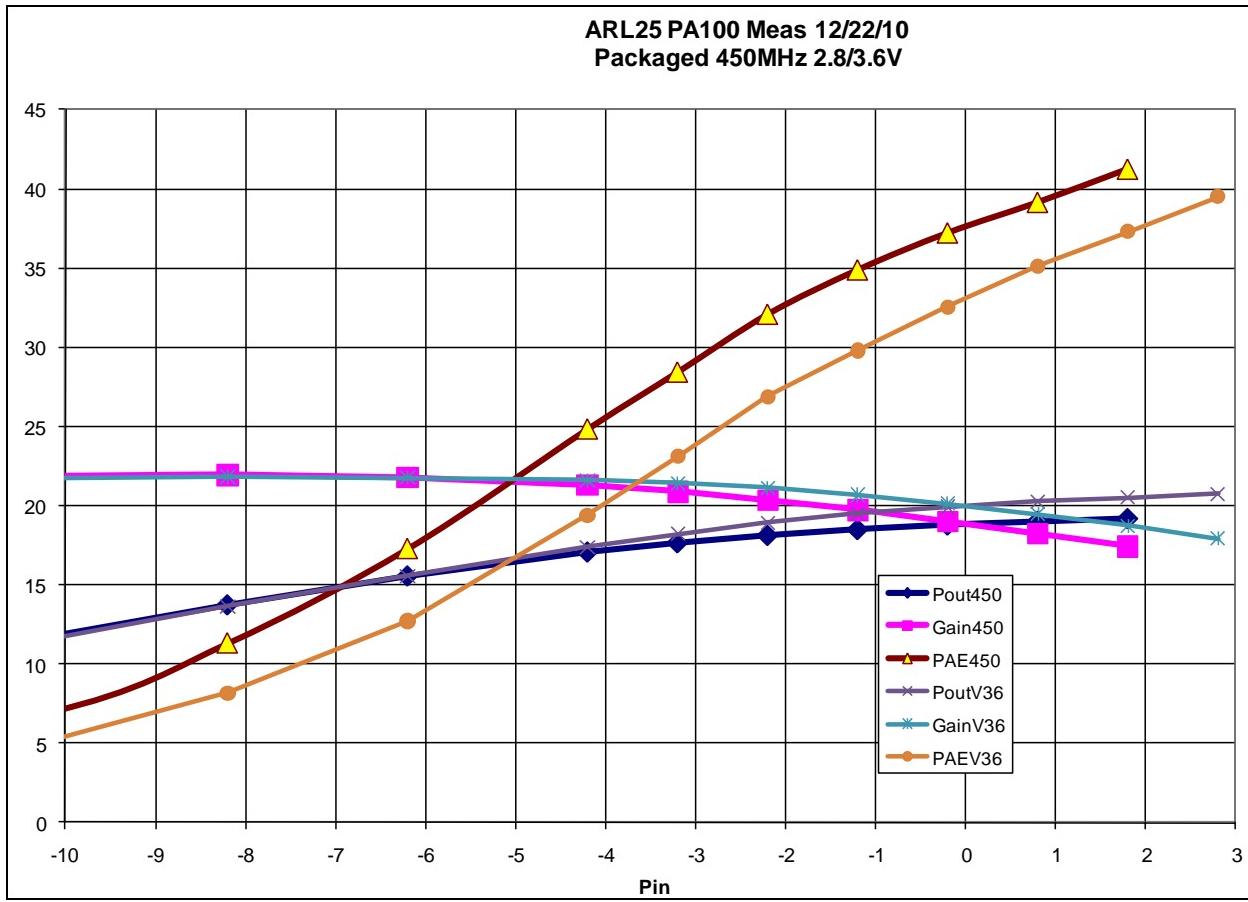


Figure 13. 100 mW PA power performance at 450 MHz (2.8/3.6V)

Table 5. 100 mW PA power performance at 500 MHz (2.8 V).

12/22/2010 Measured with Power Meter									
500 MHz	Package #1	ARL25 PA100mW ARLTILE2 TQPED				2.8V ; 76 mA			
Pin(SG)	Pout(PM)	Pin(corr)	Pout(corr)	Gain	I1(2.8V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	1.22	-20.20	1.22	21.42	76	212.8	1.32	0.6	0.6
-15.0	6.20	-15.20	6.20	21.40	76	212.8	4.17	2.0	1.9
-10.0	11.15	-10.20	11.15	21.35	75	210.0	13.03	6.2	6.2
-8.0	13.18	-8.20	13.18	21.38	74	207.2	20.80	10.0	10.0
-6.0	15.10	-6.20	15.10	21.30	74	207.2	32.36	15.6	15.5
-4.0	16.76	-4.20	16.76	20.96	73	204.4	47.42	23.2	23.0
-3.0	17.43	-3.20	17.43	20.63	73	204.4	55.34	27.1	26.8
-2.0	17.98	-2.20	17.98	20.18	72	201.6	62.81	31.2	30.9
-1.0	18.44	-1.20	18.44	19.64	72	201.6	69.82	34.6	34.3
0.0	18.81	-0.20	18.81	19.01	72	201.6	76.03	37.7	37.2
1.0	19.10	0.80	19.10	18.30	72	201.6	81.28	40.3	39.7
2.0	19.33	1.80	19.33	17.53	71	198.8	85.70	43.1	42.3

Table 6. 100 mW PA power performance at 500 MHz (3.6 V).

12/22/2010	Measured with Power Meter									
500 MHz	Package # ARL25 PA100mW ARLTILE2 TQPED					3.6V ; 79 mA				
Pin(SG)	Pout(PM)	Pin(corr)	Pout(corr)	Gain	I1(3.6V)	PDC(mw)	Pout(mw)	Drn Eff	PAE	
-20.0	1.16	-20.20	1.16	21.36	79	284.4	1.31	0.5	0.5	
-15.0	6.13	-15.20	6.13	21.33	79	284.4	4.10	1.4	1.4	
-10.0	11.08	-10.20	11.08	21.28	78	280.8	12.82	4.6	4.5	
-8.0	13.10	-8.20	13.10	21.30	78	280.8	20.42	7.3	7.2	
-6.0	15.06	-6.20	15.06	21.26	77	277.2	32.06	11.6	11.5	
-4.0	16.95	-4.20	16.95	21.15	77	277.2	49.55	17.9	17.7	
-3.0	17.84	-3.20	17.84	21.04	77	277.2	60.81	21.9	21.8	
-2.0	18.65	-2.20	18.65	20.85	78	280.8	73.28	26.1	25.9	
-1.0	19.34	-1.20	19.34	20.54	79	284.4	85.90	30.2	29.9	
0.0	19.87	-0.20	19.87	20.07	80	288.0	97.05	33.7	33.4	
1.0	20.30	0.80	20.30	19.50	81	291.6	107.15	36.7	36.3	
2.0	20.64	1.80	20.64	18.84	82	295.2	115.88	39.3	38.7	
3.0	20.90	2.80	20.90	18.10	81	291.6	123.03	42.2	41.5	

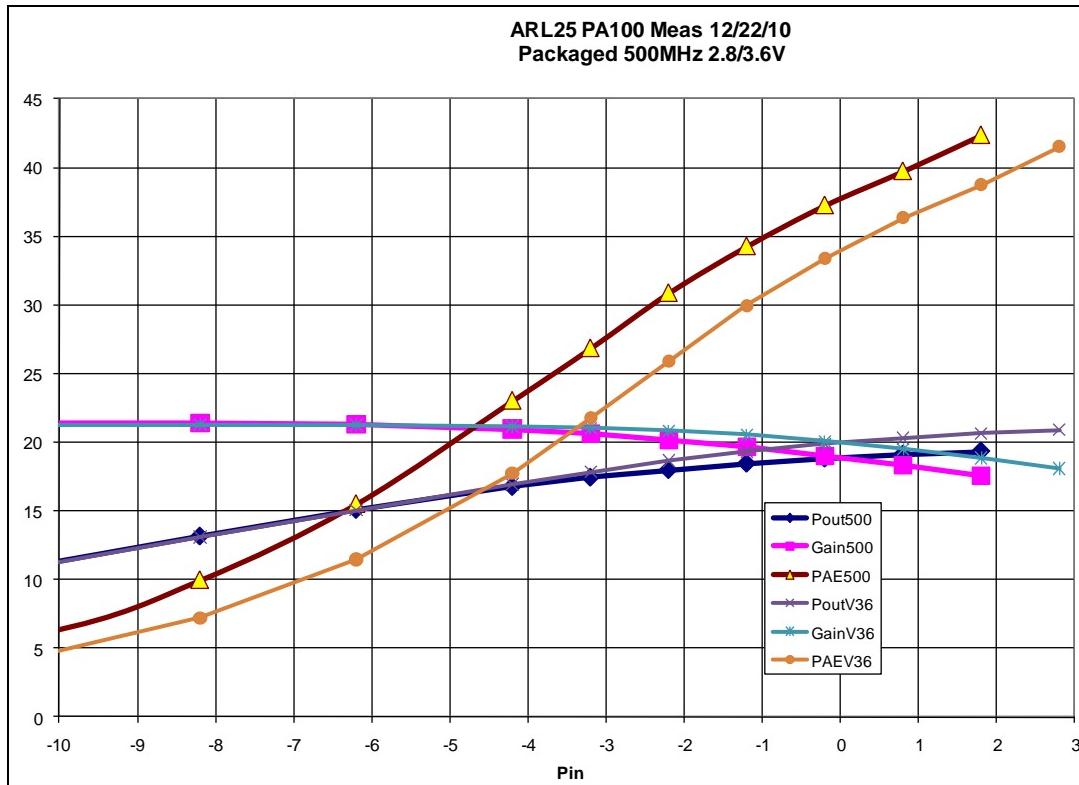


Figure 14. 100 mW PA power performance at 500 MHz (2.8/3.6 V).

50 mW Power Amplifier: I measured the RF output power of the packaged amplifier versus the input power to yield power added efficiency, gain, and DC power consumption. These measurements were performed at 2.8 V and 3.6 V, presuming a regulated power supply from either a 3.0 V battery or a 3.9 V lithium battery, at 425 MHz, and 500 MHz. Table 7 shows the measured performance at 2.8 V and 425 MHz, while table 8 is at 3.6 V. Figure 15, shows a plot

summarizing the measurements versus RF input Power. Tables 9 and 10, plus figure 16 show the performance at 500 MHz, which is slightly improved over the 425 MHz measurements. At 3 dB compression and 500 MHz, the power added efficiency is good at 37 to 38% and increases a bit at higher compression levels, i.e., higher RF input levels. At 425 MHz and 2.8 V, the 50 mW output power goal is about 0.6 dB low (43 mW), but is just achieved at 3.6 V (50 mW) with less efficiency, a mere 25% PAE. Like the 100 mW design, this amplifier had slightly lower gain and less output power than predicted from the original simulations, but some of this could be normal process variation. The efficiency of this 50 mW design was better at 2.8 V than 3.6 V and at the higher end of the 400 to 500 MHz band. Performance of this amplifier in the RF Booster ICs will be slightly less due to the 0.5 dB insertion loss of the TR switch. This design performed well at 500 MHz, but just adequately at 425 MHz. Also, the poor output return loss due to the compromise for output power and efficiency may make this design less suitable than the 100 mW design in many cases.

Table 7. 50 mW PA power performance at 425 MHz (2.8 V).

12/22/2010 Measured with Power Meter											
425 MHz	Package #1	ARL25 PA50mW ARLTILE2 TQPED				2.8V ;40 mA					
Pin(SG)	Pout(PM)	Pin(corr)	Pout(corr)	Gain	I1(2.8V)	PDC(mw)	Pout(mw)	Drn Eff	PAE		
-20.0	-1.73	-20.20	-1.73	18.47	39	109.2	0.67	0.6	0.6		
-15.0	3.20	-15.20	3.20	18.40	39	109.2	2.09	1.9	1.9		
-10.0	8.00	-10.20	8.00	18.20	40	112.0	6.31	5.6	5.5		
-8.0	9.80	-8.20	9.80	18.00	40	112.0	9.55	8.5	8.4		
-6.0	11.57	-6.20	11.57	17.77	42	117.6	14.35	12.2	12.0		
-4.0	13.20	-4.20	13.20	17.40	44	123.2	20.89	17.0	16.6		
-3.0	13.97	-3.20	13.97	17.17	46	128.8	24.95	19.4	19.0		
-2.0	14.69	-2.20	14.69	16.89	48	134.4	29.44	21.9	21.5		
-1.0	15.35	-1.20	15.35	16.55	50	140.0	34.28	24.5	23.9		
0.0	15.91	-0.20	15.91	16.11	52	145.6	38.99	26.8	26.1		
1.0	16.36	0.80	16.36	15.56	53	148.4	43.25	29.1	28.3		
2.0	16.71	1.80	16.71	14.91	53	148.4	46.88	31.6	30.6		

Table 8. 50 mW PA power performance at 425 MHz (3.6 V).

12/22/2010	Measured with Power Meter								
425 MHz	Package # ARL25 PA50mW ARLTILE2 TQPED					3.6V ; 40 mA			
Pin(SG)	Pout(PM)	Pin(corr)	Pout(corr)	Gain	I1(3.6V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-1.90	-20.20	-1.90	18.30	40	144.0	0.65	0.4	0.4
-15.0	3.02	-15.20	3.02	18.22	40	144.0	2.00	1.4	1.4
-10.0	7.85	-10.20	7.85	18.05	41	147.6	6.10	4.1	4.1
-8.0	9.64	-8.20	9.64	17.84	42	151.2	9.20	6.1	6.0
-6.0	11.42	-6.20	11.42	17.62	43	154.8	13.87	9.0	8.8
-4.0	13.07	-4.20	13.07	17.27	45	162.0	20.28	12.5	12.3
-3.0	13.83	-3.20	13.83	17.03	47	169.2	24.15	14.3	14.0
-2.0	14.55	-2.20	14.55	16.75	49	176.4	28.51	16.2	15.8
-1.0	15.23	-1.20	15.23	16.43	51	183.6	33.34	18.2	17.7
0.0	15.88	-0.20	15.88	16.08	53	190.8	38.73	20.3	19.8
1.0	16.44	0.80	16.44	15.64	54	194.4	44.06	22.7	22.0
2.0	16.95	1.80	16.95	15.15	56	201.6	49.55	24.6	23.8
3.0	17.37	2.80	17.37	14.57	56	201.6	54.58	27.1	26.1

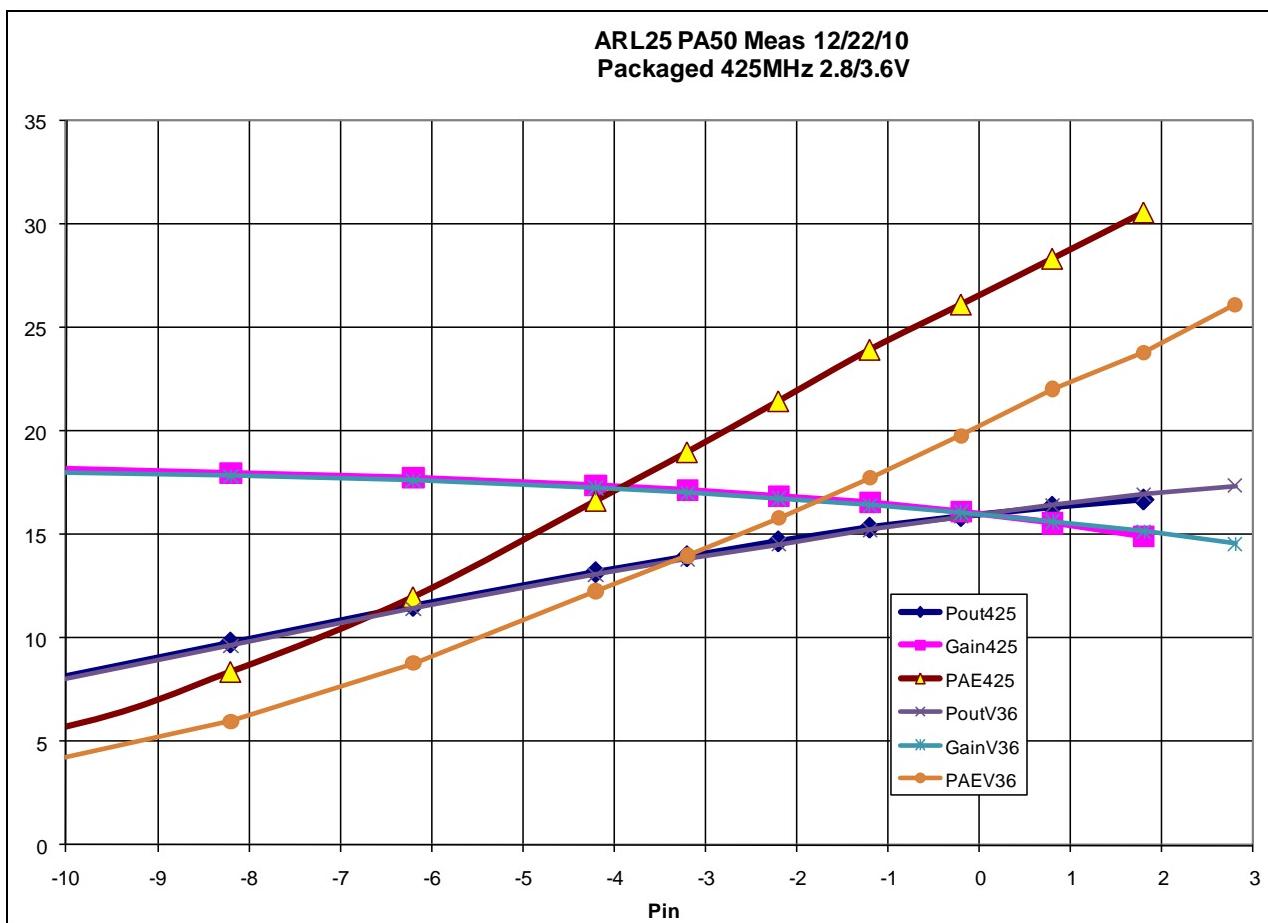


Figure 15. 50 mW PA power performance at 425 MHz (2.8/3.6 V).

Table 9. 50 mW PA power performance at 500 MHz (2.8 V).

12/22/2010 Measured with Power Meter		500 MHz Package #1 ARL25 PA50mW ARLTILE2 TQPED				2.8V ;40 mA			
Pin(SG)	Pout(PM)	Pin(corr)	Pout(corr)	Gain	I1(2.8V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-1.10	-20.20	-1.10	19.10	39	109.2	0.78	0.7	0.7
-15.0	3.82	-15.20	3.82	19.02	39	109.2	2.41	2.2	2.2
-10.0	8.69	-10.20	8.69	18.89	39	109.2	7.40	6.8	6.7
-8.0	10.56	-8.20	10.56	18.76	40	112.0	11.38	10.2	10.0
-6.0	12.42	-6.20	12.42	18.62	41	114.8	17.46	15.2	15.0
-4.0	14.16	-4.20	14.16	18.36	43	120.4	26.06	21.6	21.3
-3.0	14.95	-3.20	14.95	18.15	44	123.2	31.26	25.4	25.0
-2.0	15.66	-2.20	15.66	17.86	46	128.8	36.81	28.6	28.1
-1.0	16.26	-1.20	16.26	17.46	47	131.6	42.27	32.1	31.5
0.0	16.75	-0.20	16.75	16.95	49	137.2	47.32	34.5	33.8
1.0	17.14	0.80	17.14	16.34	50	140.0	51.76	37.0	36.1
2.0	17.43	1.80	17.43	15.63	50	140.0	55.34	39.5	38.4

Table 10. 50 mW PA power performance at 500 MHz (3.6 V).

12/22/2010 Measured with Power Meter		500 MHz Package # ARL25 PA50mW ARLTILE2 TQPED				3.6V ; 40 mA			
Pin(SG)	Pout(PM)	Pin(corr)	Pout(corr)	Gain	I1(3.6V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-1.27	-20.20	-1.27	18.93	40	144.0	0.75	0.5	0.5
-15.0	3.65	-15.20	3.65	18.85	40	144.0	2.32	1.6	1.6
-10.0	8.53	-10.20	8.53	18.73	41	147.6	7.13	4.8	4.8
-8.0	10.41	-8.20	10.41	18.61	41	147.6	10.99	7.4	7.3
-6.0	12.26	-6.20	12.26	18.46	42	151.2	16.83	11.1	11.0
-4.0	14.03	-4.20	14.03	18.23	43	154.8	25.29	16.3	16.1
-3.0	14.85	-3.20	14.85	18.05	45	162.0	30.55	18.9	18.6
-2.0	15.62	-2.20	15.62	17.82	46	165.6	36.48	22.0	21.7
-1.0	16.35	-1.20	16.35	17.55	48	172.8	43.15	25.0	24.5
0.0	17.01	-0.20	17.01	17.21	50	180.0	50.23	27.9	27.4
1.0	17.58	0.80	17.58	16.78	52	187.2	57.28	30.6	30.0
2.0	18.04	1.80	18.04	16.24	53	190.8	63.68	33.4	32.6
3.0	18.40	2.80	18.40	15.60	54	194.4	69.18	35.6	34.6

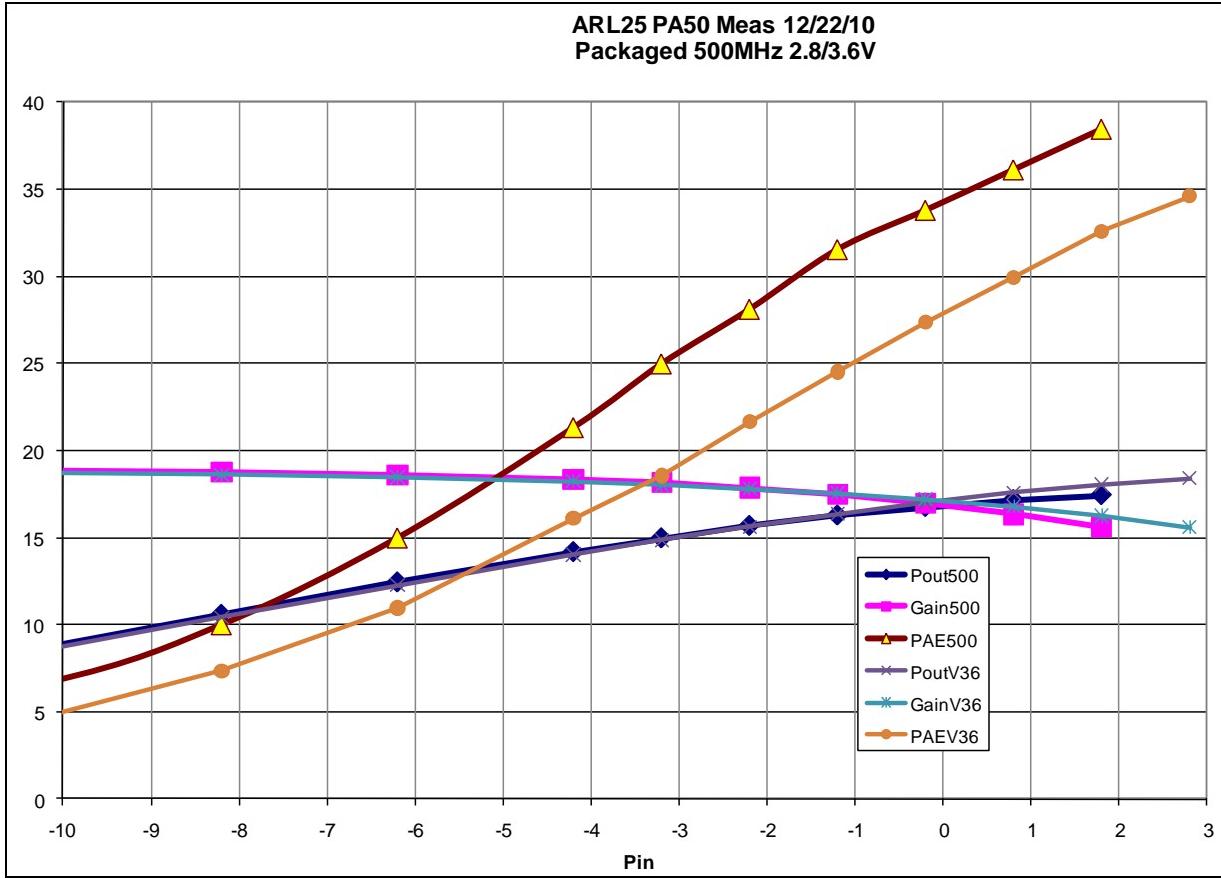


Figure 16. 50 mW PA power performance at 500 MHz (2.8/3.6 V).

Low Noise Amplifier: The noise figure and gain of the packaged low noise amplifier was measured as shown in table 11. Even by adding 0.2 dB to the gain and subtracting 0.1 dB from the noise figure to adjust for the loss of the PC board and the SMA connectors, a higher than expected noise figure still exists, about 0.75 dB higher than predicted. The 10 dB gain was also about 2 dB lower than predicted by simulations, but otherwise the performance and low DC power consumption of the low noise amplifier was very good. Normal process variation may explain some of the discrepancies. Performance of this low noise amplifier within the RF Booster ICs will be slightly less due to the 0.5 dB insertion loss of the TR switch at the input, so the noise figure should increase slightly and the gain should be reduced.

Table 11. LNA noise figure performance at 2.8 V and 3 mA DC bias.

Meas 12/28/10		Packaged LNA 2.8V 3	
LNA	Freq	Gain	NF
ARL25B	400	8.97	3.23
SMA	450	9.83	2.95
w/ caps	500	9.83	2.90
	550	8.73	3.00

ARL21M425 RFIC: This 425 MHz Booster IC design consists of a TR Switch, a BPSK modulator, a 100 mW power amplifier, and a low current low noise amplifier (figure 17). S-parameter measurements were made of the transmit and receive modes as well as performance measurements. Isolation from the TR switch was measured with the TR switch in receive mode, while measuring the transmit isolation, similarly for the transmit mode isolation. There was little change in performance at 2.8 V versus 3.6 V, as the designs are intended to be robust over a battery supply range of about 2 V up to 5 V (even 6 V or higher is possible at reduced efficiency).

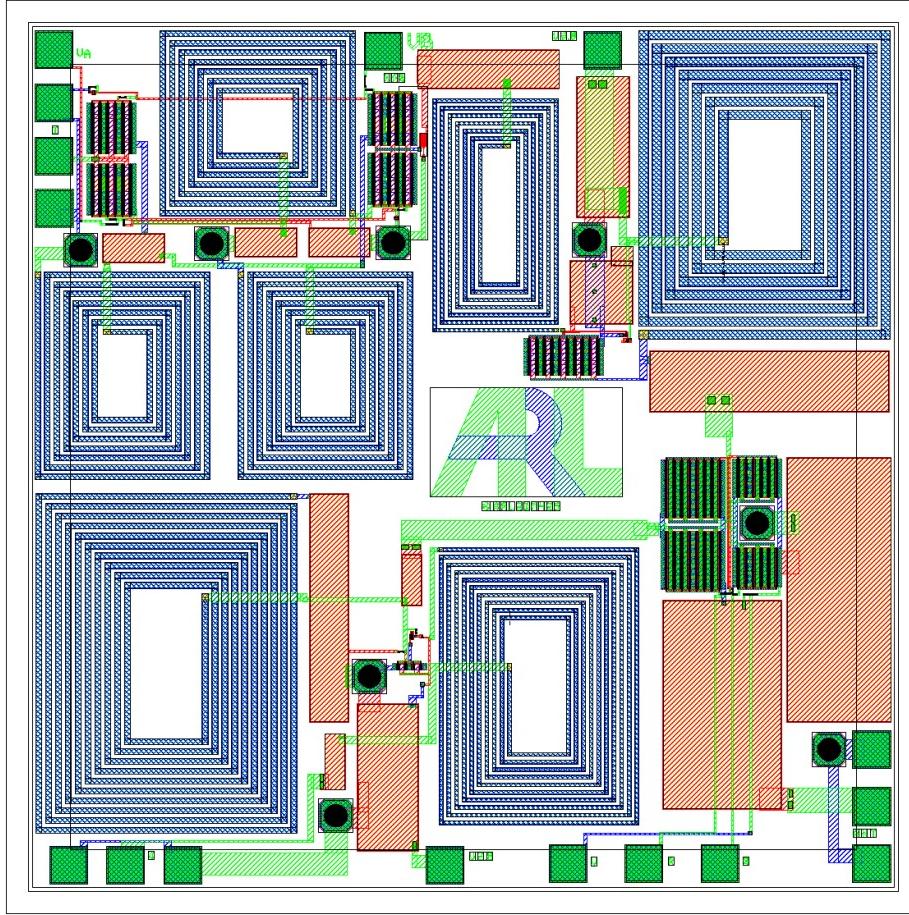


Figure 17. Plot of ARL21M425 test chip (BPSK, 100 mW PA, LNA, & TRS).

Figure 18 shows just over 19 dB gain for the high pass and low pass states of the BPSK modulator with about 43 dB of isolation for the transmit path when switched to receive. Figure 19 shows the relative phase shift between the two BPSK states—which is very close to the ideal 180 degrees at 425 MHz. Input return loss (figure 20) is good for the transmit state, and even in the isolation/receive mode. Output return loss (figure 21) is better than 12 dB for the transmit state, and is a little worse in the isolation/receive mode.

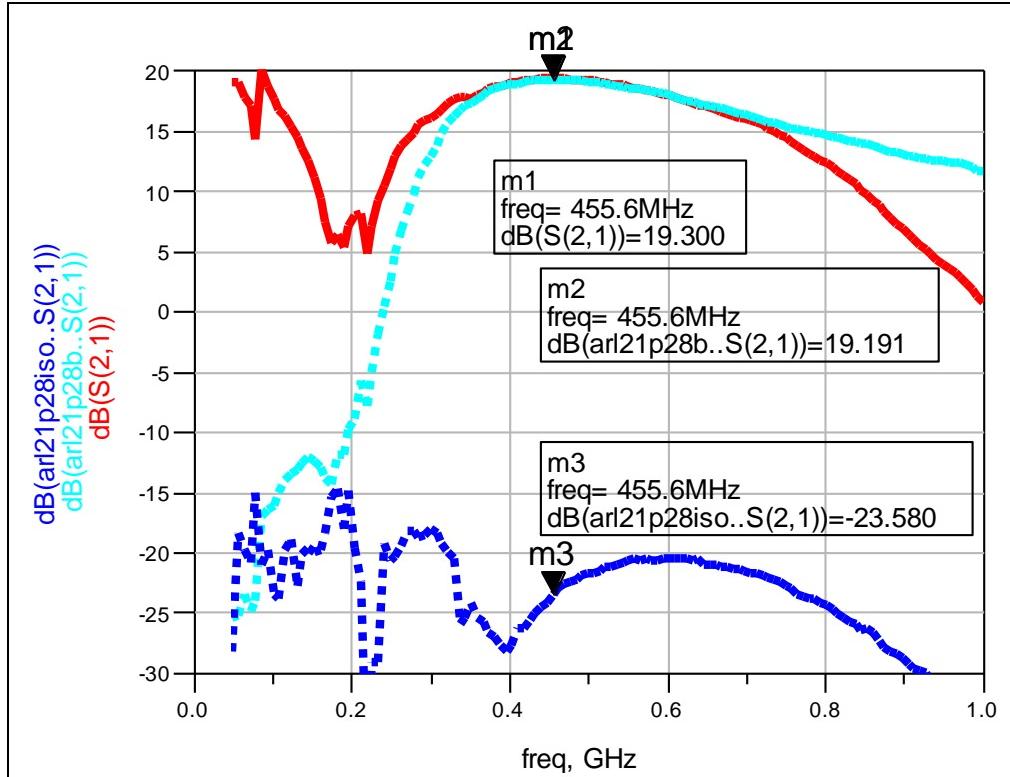


Figure 18. Transmit gain/isolation S21 in package (ARL21M425 at 2.8 V).

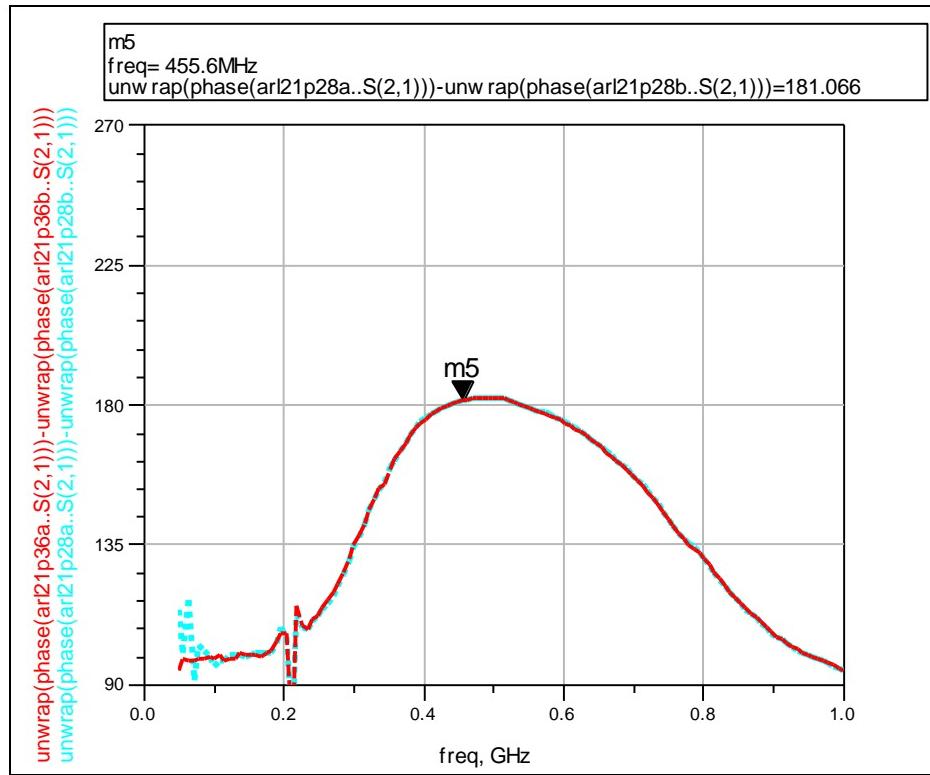


Figure 19. Relative BPSK transmit phase S21 in package (ARL21M425 at 2.8/3.6 V).

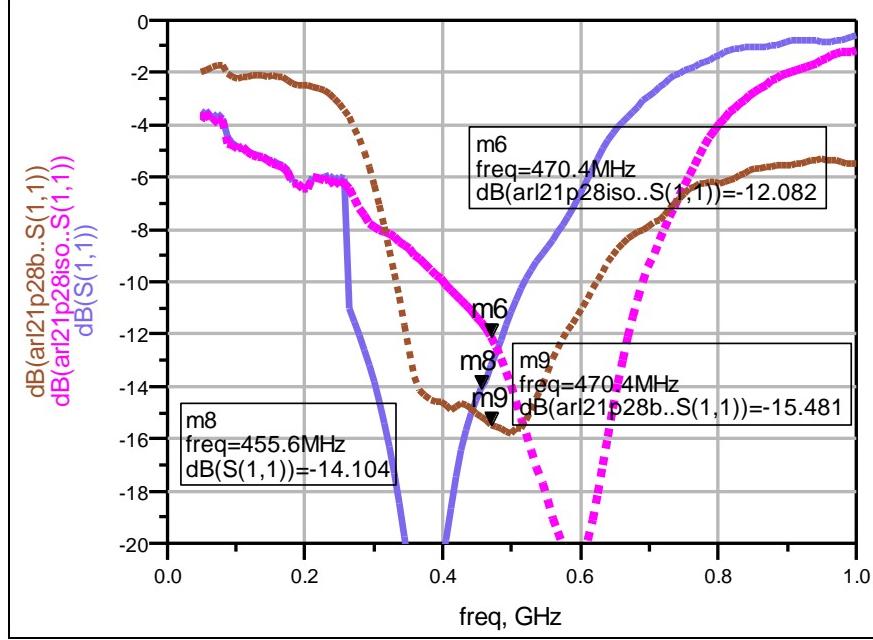


Figure 20. Transmit input return loss S11 in package (ARL21M425 at 2.8 V).

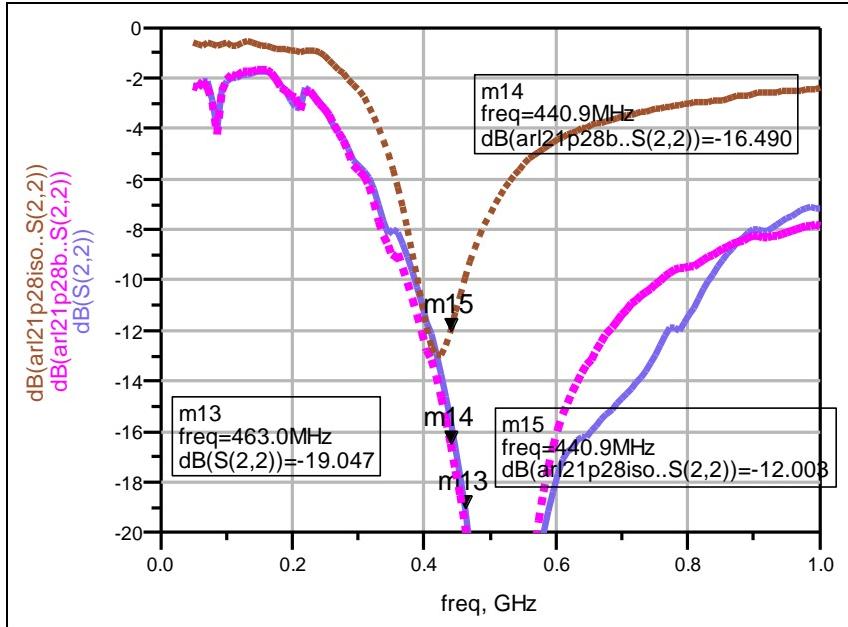


Figure 21. Transmit output return loss S22 in package (ARL21M425 at 2.8 V).

For the receive state, figure 22 shows just over 10 dB gain for the low noise amplifier and TR switch loss, with about 42 dB of isolation for the receive path when switched to transmit. Input return loss (figure 23) is a decent 10 dB for the receive state, and even better in the isolation/transmit mode. Output return loss (figure 24) is very good at 17 dB for the receive state, and is about the same in the isolation/transmit mode.

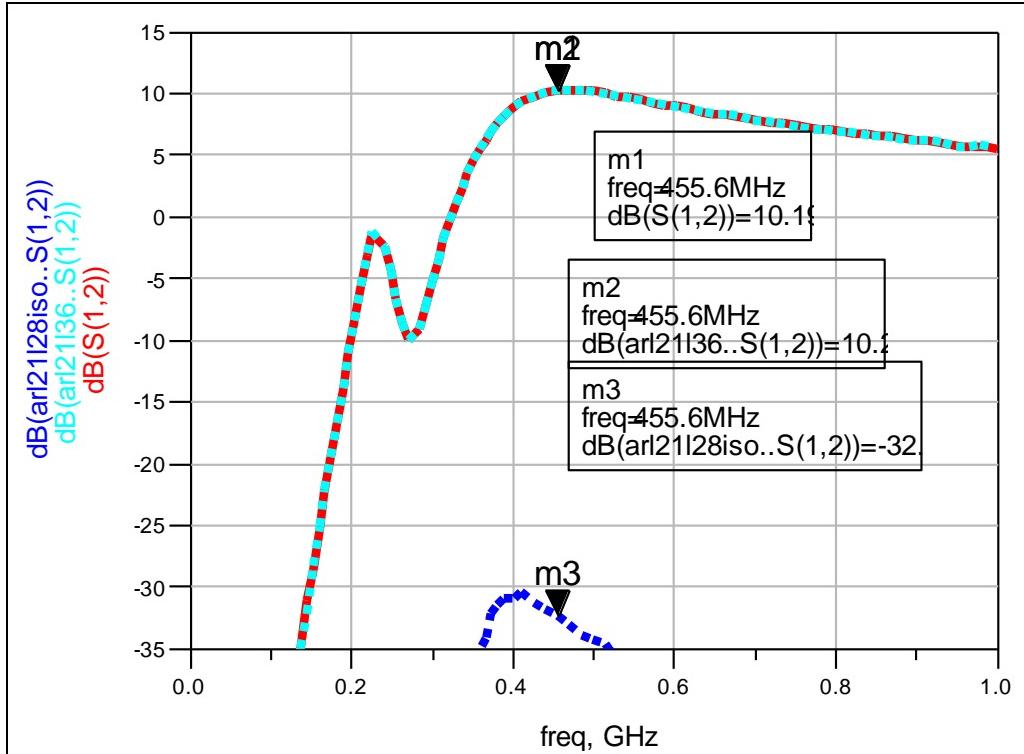


Figure 22. Transmit gain/isolation S21 in package (ARL21M425 at 2.8 V).

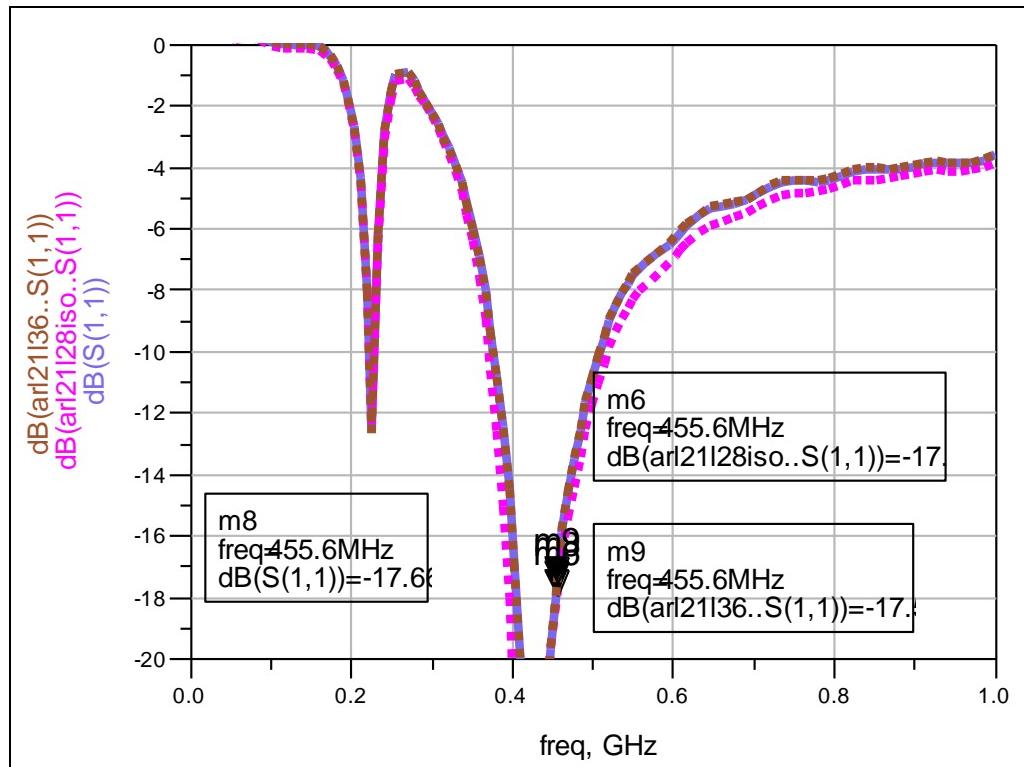


Figure 23. Receive output return loss in package (ARL21M425 at 2.8 V).

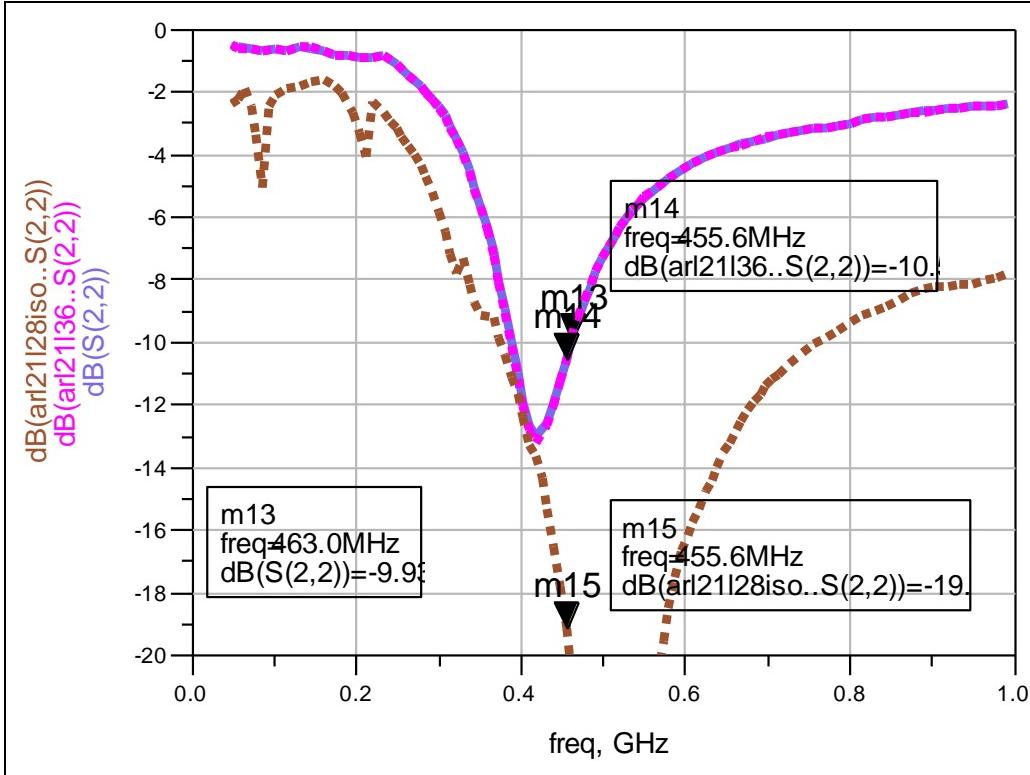


Figure 24. Receive input return loss in package (ARL21M425 at 2.8 V).

ARL21M425 Performance: While switched to the transmit path, I measured the RF output power of the packaged Booster IC versus the input power to yield power added efficiency, gain, and DC power consumption. These measurements were performed at 2.8 V and 3.6 V, presuming a regulated power supply from either a 3.0 V battery or a 3.9 V lithium battery, at 425 MHz, and 500 MHz. Table 12 shows the measured performance at 2.8 V and 425 MHz, while table 13 is at 3.6V. Figure 25, shows a plot summarizing the measurements versus RF input Power. Tables 14 and 15, plus figure 26 show the performance at 500 MHz which is improved compared to 425 MHz. At 3 dB compression and 425 MHz, the power added efficiency is good at 37% and increases a bit at higher compression levels, i.e., higher RF input levels. At 425 MHz and 2.8 V, the output power is about 70 mW, but is about 100 mW at 3.6 V, also with 37% PAE. The performance of this RF Booster IC is comparable to the standalone 100 mW amplifier of the ARL25 test chip plus about 2 dB insertion loss at the input. This is due to the BPSK modulator and the 0.5 dB insertion loss of the TR switch on the output. This design performed slightly better at 500 MHz and had similar efficiency (PAE) at 2.8 V versus 3.6 V with greater output power at 3.6 V. On the receive side, I measured the noise figure and gain were measured at 450 MHz to be 10.8 dB and 3.7 dB respectively. The gain was about as expected but the noise figure was about 1 dB higher than that predicted by simulations.

Table 12. ARL21M425 power performance at 425 MHz (2.8 V).

Measured with Power Meter									
425 MHz	Package #1		2.8V ; 78 mA						
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(2.8V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-1.03	-20.20	-1.03	19.17	78	218.4	0.79	0.4	0.4
-10.0	8.89	-10.20	8.89	19.09	77	215.6	7.74	3.6	3.5
-8.0	11.09	-8.20	11.09	19.29	77	215.6	12.85	6.0	5.9
-6.0	13.04	-6.20	13.04	19.24	76	212.8	20.14	9.5	9.4
-4.0	14.92	-4.20	14.92	19.12	75	210.0	31.05	14.8	14.6
-2.0	16.53	-2.20	16.53	18.73	73	204.4	44.98	22.0	21.7
0.0	17.68	-0.20	17.68	17.88	70	196.0	58.61	29.9	29.4
1.0	18.08	0.80	18.08	17.28	69	193.2	64.27	33.3	32.6
2.0	18.37	1.80	18.37	16.57	68	190.4	68.71	36.1	35.3
3.0	18.59	2.80	18.59	15.79	67	187.6	72.28	38.5	37.5
4.0	18.73	3.80	18.73	14.93	65	182.0	74.64	41.0	39.7
5.0	18.83	4.80	18.83	14.03	62	173.6	76.38	44.0	42.3

Table 13. ARL21M425 power performance at 425 MHz (3.6 V).

Measured with Power Meter									
425 MHz	Package #1		3.6V ; 81 mA						
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(3.6V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-1.10	-20.20	-1.10	19.10	81	291.6	0.78	0.3	0.3
-10.0	8.82	-10.20	8.82	19.02	80	288.0	7.62	2.6	2.6
-8.0	11.01	-8.20	11.01	19.21	80	288.0	12.62	4.4	4.3
-6.0	12.96	-6.20	12.96	19.16	79	284.4	19.77	7.0	6.9
-4.0	14.88	-4.20	14.88	19.08	78	280.8	30.76	11.0	10.8
-2.0	16.70	-2.20	16.70	18.90	77	277.2	46.77	16.9	16.7
0.0	18.30	-0.20	18.30	18.50	76	273.6	67.61	24.7	24.4
1.0	18.91	0.80	18.91	18.11	76	273.6	77.80	28.4	28.0
2.0	19.37	1.80	19.37	17.57	76	273.6	86.50	31.6	31.1
3.0	19.73	2.80	19.73	16.93	76	273.6	93.97	34.3	33.7
4.0	19.99	3.80	19.99	16.19	75	270.0	99.77	37.0	36.1
5.0	20.17	4.80	20.17	15.37	73	262.8	103.99	39.6	38.4

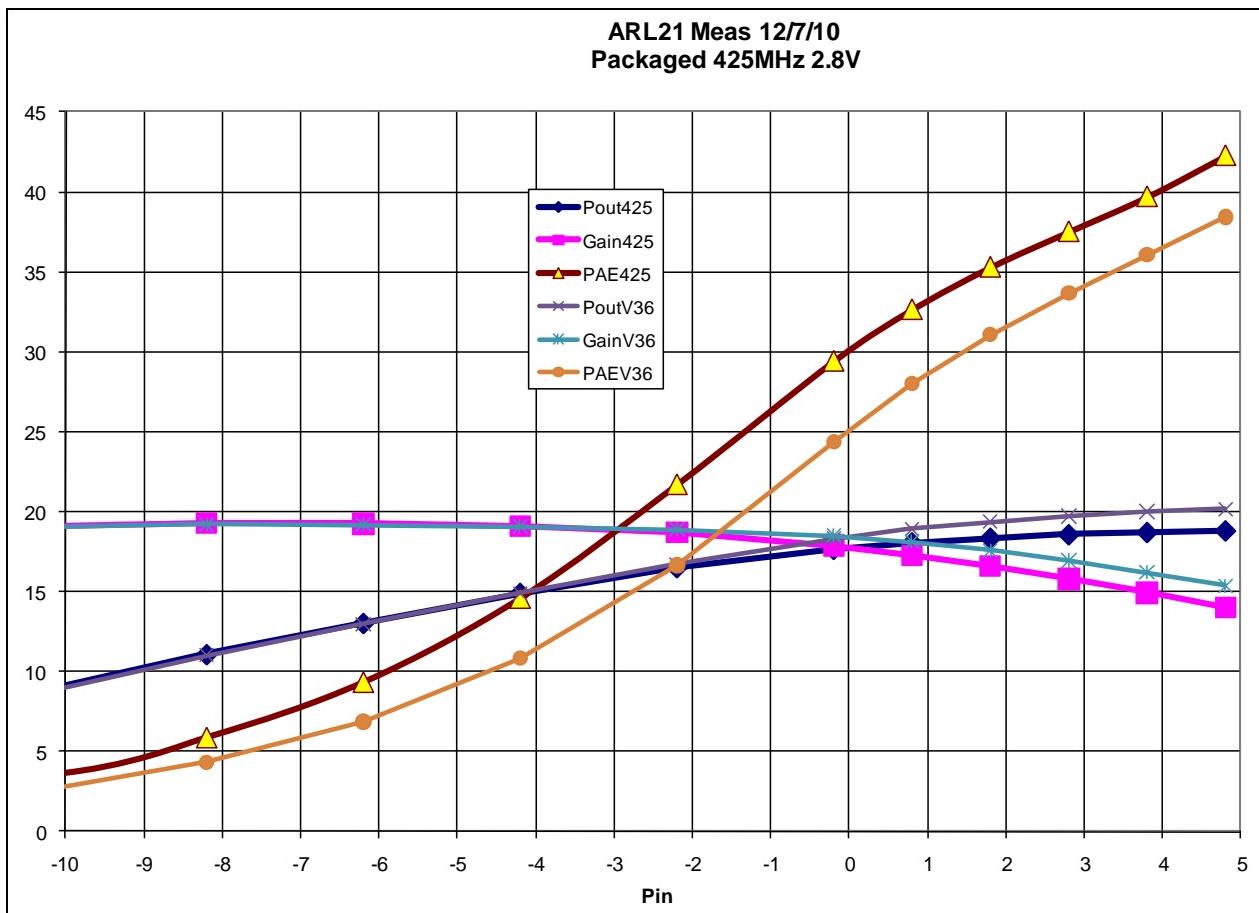


Figure 25. ARL21M425 power performance at 425 MHz (2.8/3.6 V).

Table 14. ARL21M425 power performance at 500 MHz (2.8 V).

12/7/2010 Measured with Power Meter									
500 MHz	Package #1			2.8V ; 78 mA					
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(2.8V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-1.33	-20.20	-1.33	18.87	78	218.4	0.74	0.3	0.3
-10.0	8.66	-10.20	8.66	18.86	77	215.6	7.35	3.4	3.4
-8.0	10.76	-8.20	10.76	18.96	77	215.6	11.91	5.5	5.5
-6.0	12.75	-6.20	12.75	18.95	76	212.8	18.84	8.9	8.7
-4.0	14.68	-4.20	14.68	18.88	75	210.0	29.38	14.0	13.8
-2.0	16.36	-2.20	16.36	18.56	73	204.4	43.25	21.2	20.9
0.0	17.63	-0.20	17.63	17.83	69	193.2	57.94	30.0	29.5
1.0	18.10	0.80	18.10	17.30	67	187.6	64.57	34.4	33.8
2.0	18.46	1.80	18.46	16.66	65	182.0	70.15	38.5	37.7
3.0	18.73	2.80	18.73	15.93	64	179.2	74.64	41.7	40.6
4.0	18.92	3.80	18.92	15.12	63	176.4	77.98	44.2	42.8
5.0	19.03	4.80	19.03	14.23	61	170.8	79.98	46.8	45.1

Table 15. ARL21M425 power performance at 500 MHz (3.6 V).

500 MHz	Package #1					3.6V ; 81 mA			
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(3.6V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-1.30	-20.20	-1.30	18.90	81	291.6	0.74	0.3	0.3
-10.0	8.67	-10.20	8.67	18.87	80	288.0	7.36	2.6	2.5
-8.0	10.78	-8.20	10.78	18.98	80	288.0	11.97	4.2	4.1
-6.0	12.76	-6.20	12.76	18.96	79	284.4	18.88	6.6	6.6
-4.0	14.74	-4.20	14.74	18.94	78	280.8	29.79	10.6	10.5
-2.0	16.62	-2.20	16.62	18.82	76	273.6	45.92	16.8	16.6
0.0	18.33	-0.20	18.33	18.53	75	270.0	68.08	25.2	24.9
1.0	19.03	0.80	19.03	18.23	74	266.4	79.98	30.0	29.6
2.0	19.58	1.80	19.58	17.78	74	266.4	90.78	34.1	33.5
3.0	19.98	2.80	19.98	17.18	73	262.8	99.54	37.9	37.2
4.0	20.28	3.80	20.28	16.48	73	262.8	106.66	40.6	39.7
5.0	20.49	4.80	20.49	15.69	72	259.2	111.94	43.2	42.0

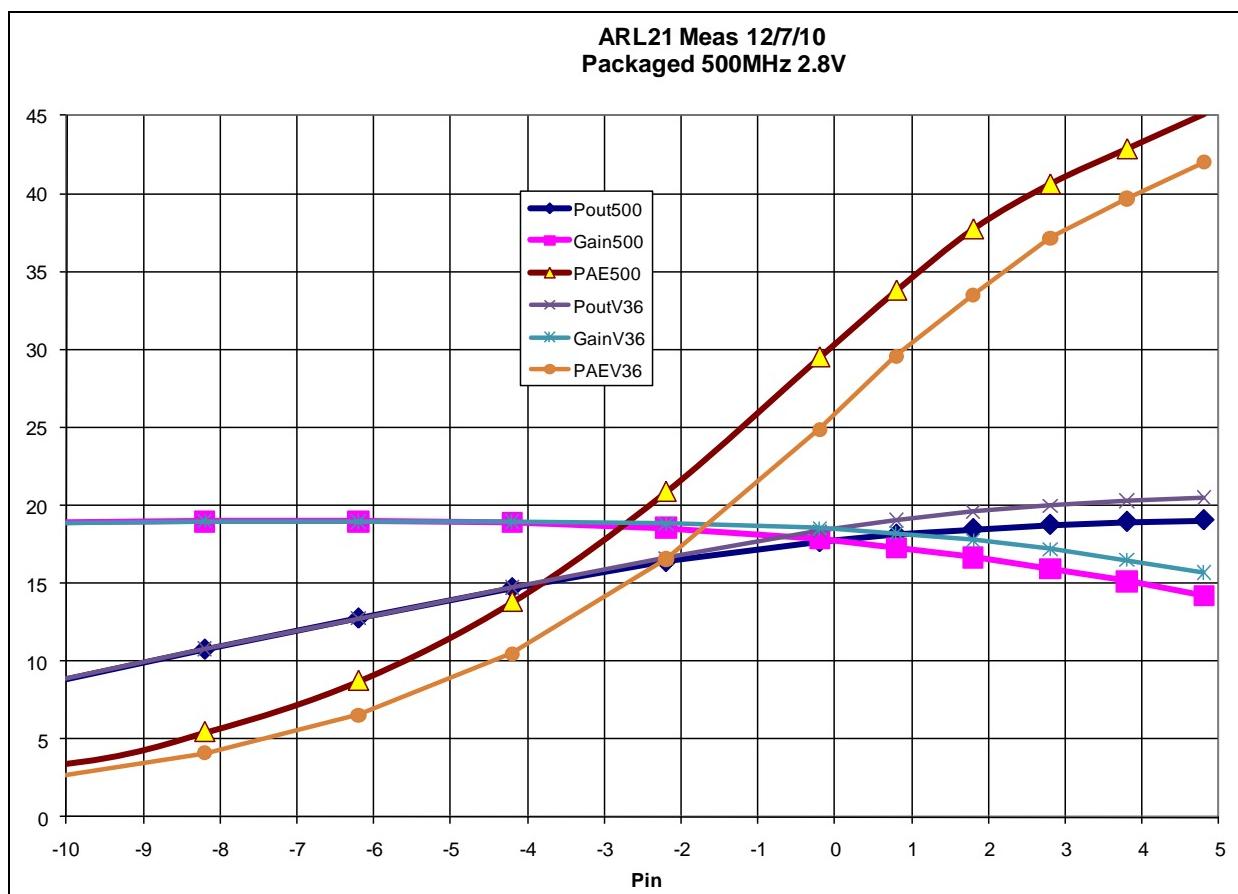


Figure 26. ARL21M425 power performance at 500 MHz (2.8/3.6 V).

ARL22M425 RFIC: This 425 MHz Booster IC design consists of a TR Switch, a BPSK modulator, a 50 mW power amplifier, and a low current low noise amplifier (figure 27). S-parameter measurements were made of the transmit and receive modes as well as performance measurements. Isolation from the TR switch was measured with the TR switch in receive mode

while measuring the transmit isolation, similarly for the transmit mode isolation. There was little change in performance at 2.8 V versus 3.6 V, as the designs are intended to be robust over a battery supply range of about 2 V up to 5 V (even 6 V or higher is possible with reduced efficiency).

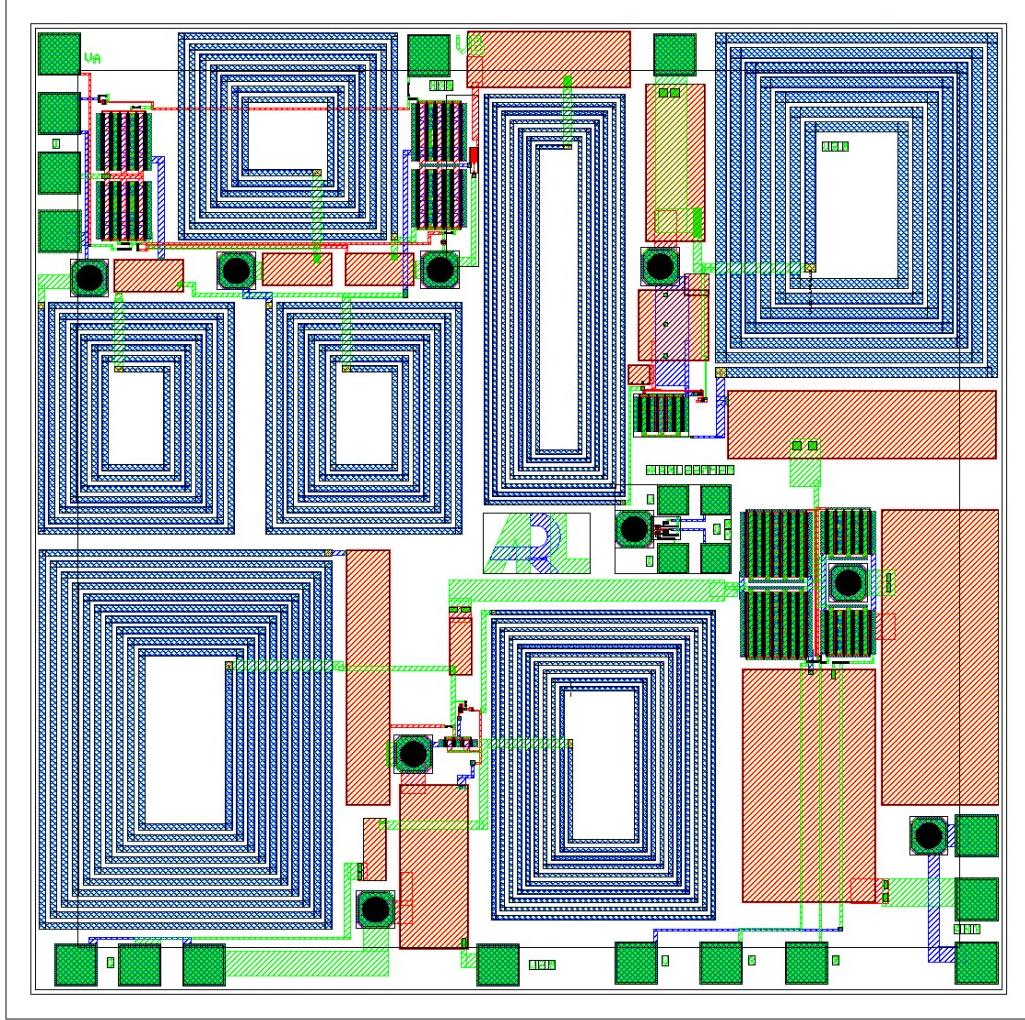


Figure 27. Plot of ARL22M425 test chip (BPSK, 50 mW PA, LNA, & TRS).

Figure 28 shows about 16 dB gain for the high pass and low pass states of the BPSK modulator with about 43 dB of isolation for the transmit path when switched to receive. Figure 29 shows the relative phase shift between the two BPSK states—which is very close to the ideal 180 degrees at 450 MHz. Input return loss (figure 30) is good for the transmit state, and even in the isolation/receive mode. Output return loss (figure 31) is a poor 6 dB for the transmit state due to the compromise match for output power over return loss. Return loss is a little better in the isolation/receive mode.

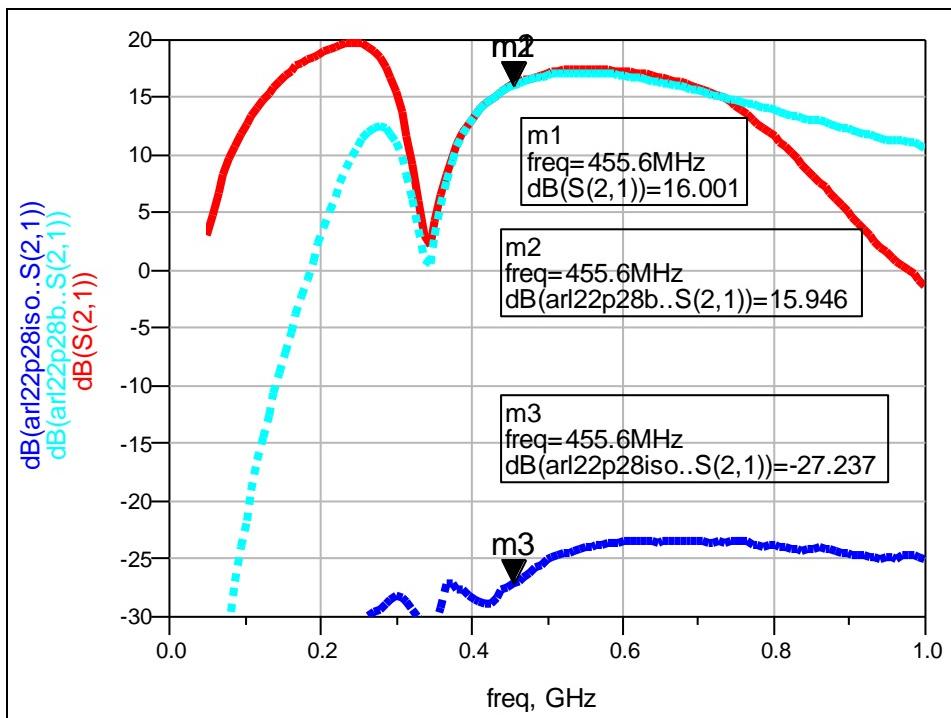


Figure 28. Transmit gain/isolation S21 in package (ARL22M425 at 2.8 V).

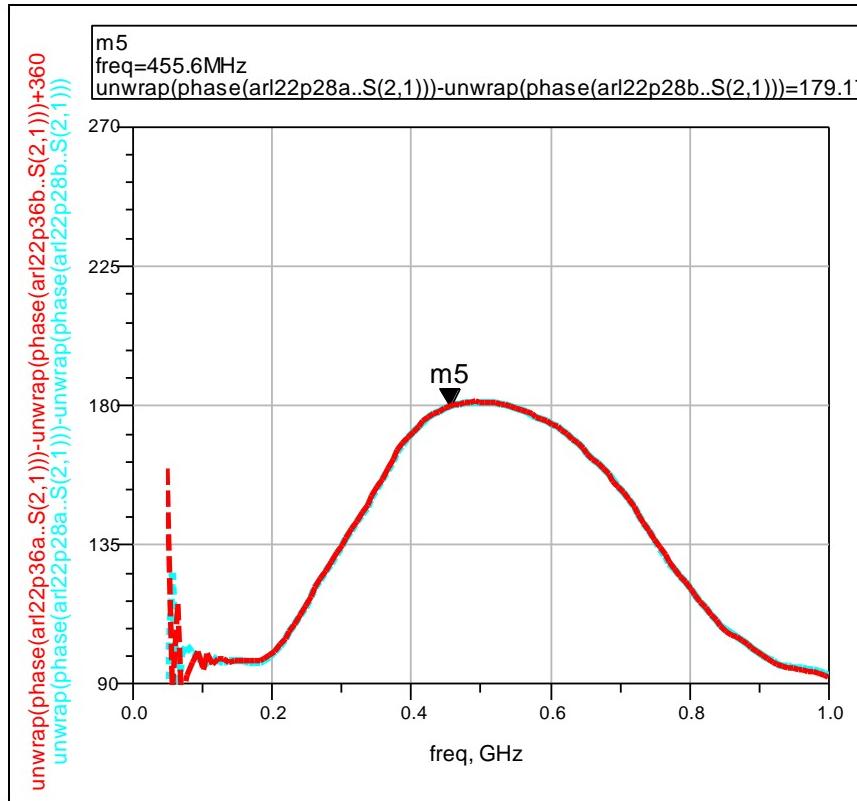


Figure 29. Relative BPSK transmit phase S21 in package (ARL22M425 at 2.8/3.6 V).

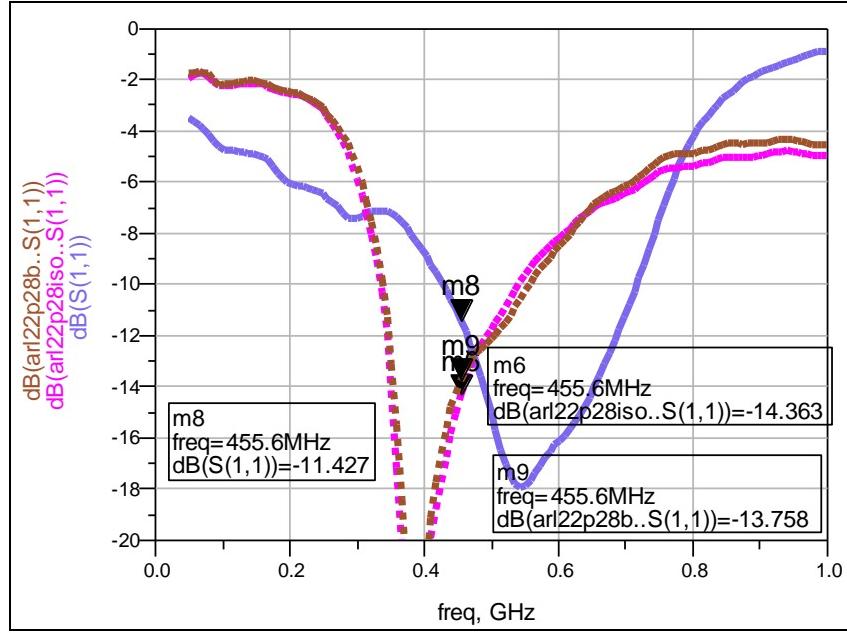


Figure 30. Transmit input return loss S11 in package (ARL22M425 at 2.8 V).

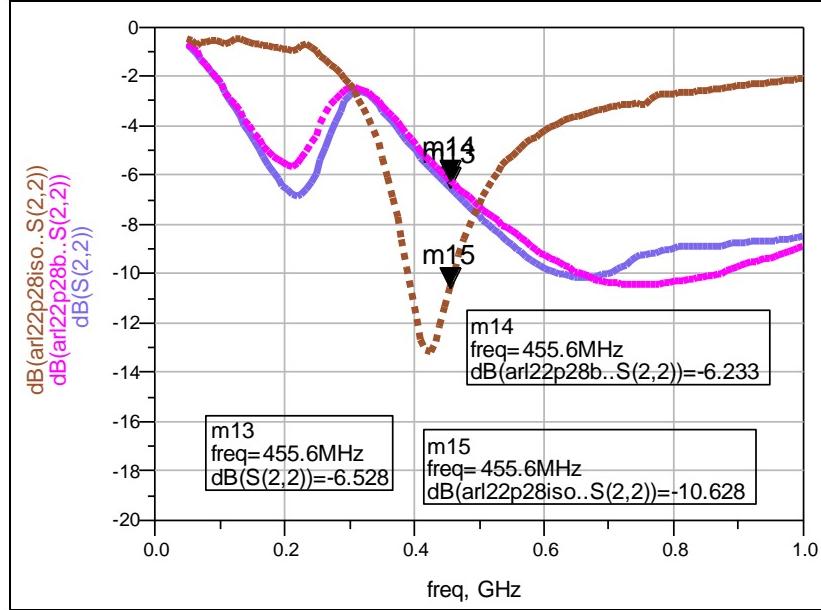


Figure 31. Transmit output return loss S22 in package (ARL22M425 at 2.8 V).

For the receive state, figure 32 shows over 10 dB gain for the low noise amplifier and TR switch loss, with about 40 dB of isolation for the receive path when switched to transmit. Input return loss (figure 33) is a decent 10 dB for the receive state, but is worse when in the isolation/transmit mode. Output return loss (figure 34) is very good at 17 dB for the receive state, and is about the same in the isolation/transmit mode.

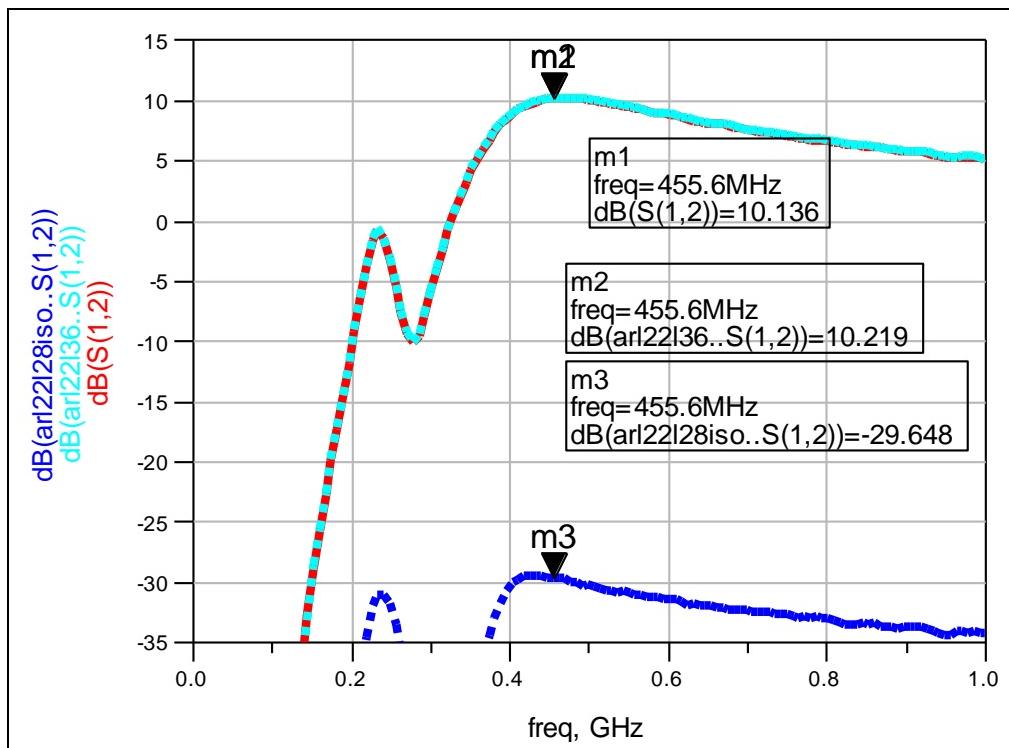


Figure 32. Transmit gain/isolation S21 in package (ARL22M425 at 2.8 V).

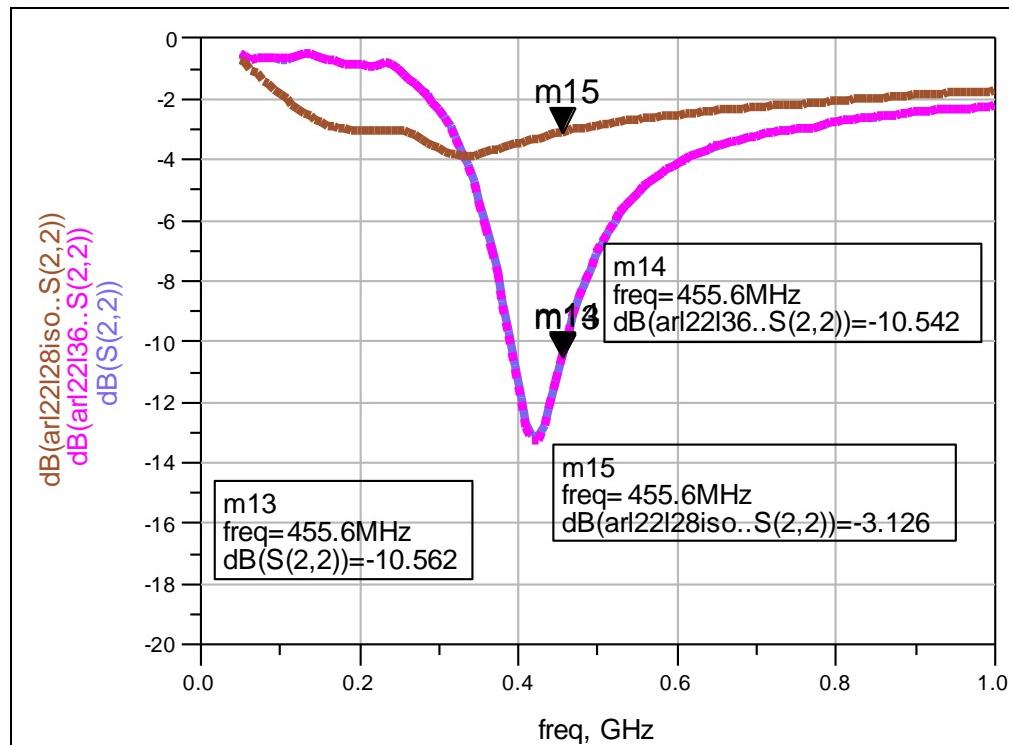


Figure 33. Receive input return loss in package (ARL22M425 at 2.8 V).

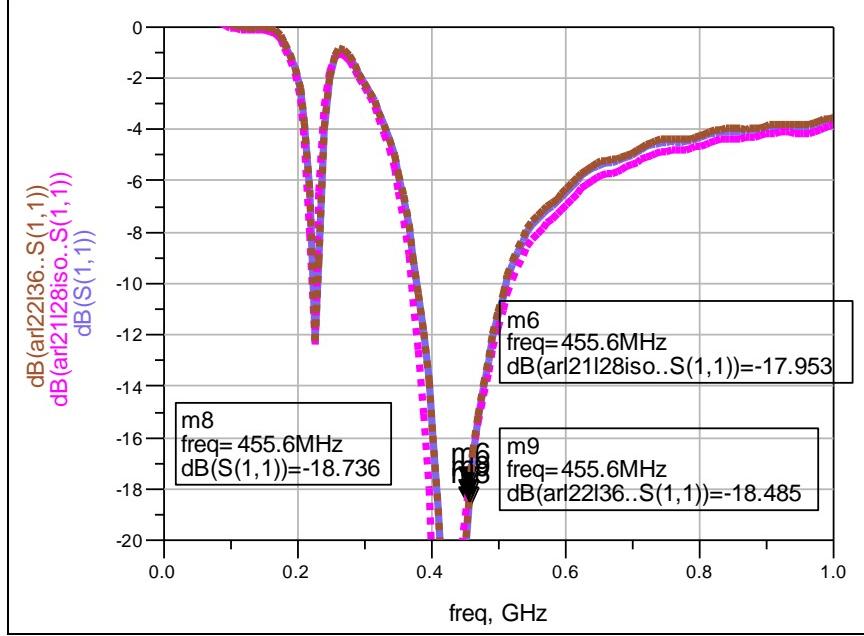


Figure 34. Receive output return loss in package (ARL22M425 at 2.8 V).

ARL22M425 Performance: While switched to the transmit path, I measured the RF output power of the packaged Booster IC versus the input power to yield power added efficiency, gain, and DC power consumption. These measurements were performed at 2.8 V and 3.6 V, presuming a regulated power supply from either a 3.0 V battery or a 3.9 V lithium battery, at 425 MHz, 500 MHz, and 600 MHz. Table 16 shows the measured performance at 2.8 V and 425 MHz, while table 17 is at 3.6 V. Figure 35, shows a plot summarizing the measurements versus RF input Power. Tables 18 and 19, plus figure 36 show the performance at 500 MHz which is much improved over 425 MHz. At 600 MHz, the power performance is even better, as shown in tables 20, 21, with figure 37 summarizing the power performance. Possibly the design needs some re-tuning to get comparable performance in the middle of the desired band. At 3 dB compression and 425 MHz, the power added efficiency is only 27% and increases a bit at higher compression levels, i.e., higher RF input levels. At 425 MHz and 2.8 V, the output power is only 38 mW, but is no higher at 3.6 V, with even worse efficiency. The performance of this RF Booster IC is not as good as hoped from the simulations, but is comparable to the standalone 50 mW amplifier of the ARL25 test chip plus 2 dB insertion loss at the input. This is due to the BPSK modulator and the 0.5 dB insertion loss of the TR switch on the output. This design performed much better at 500 MHz, and also at 600 MHz which is probably outside the desired band of operation. At 3 dB compression and 500 MHz, the output power was 50 mW with a good 40% PAE. On the receive side, the noise figure and gain were measured at 450 MHz to be 10.6 dB and 4.5 dB, respectively. The gain was about as expected, but the noise figure was much higher than that predicted by simulations, and is considerably higher than the identical receive configuration for ARL21M425. It would probably be good to re-measure another packaged example of ARL22M425.

Table 16. ARL22M425 power performance at 425 MHz (2.8 V).

12/7/2010 Measured with Power Meter									
425 MHz	Package #1	2.8V ; 39 mA							
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(2.8V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-5.47	-20.20	-5.47	14.73	39	109.2	0.28	0.3	0.3
-10.0	4.41	-10.20	4.41	14.61	40	112.0	2.76	2.5	2.4
-8.0	6.60	-8.20	6.60	14.80	40	112.0	4.57	4.1	3.9
-6.0	8.48	-6.20	8.48	14.68	40	112.0	7.05	6.3	6.1
-4.0	10.27	-4.20	10.27	14.47	41	114.8	10.64	9.3	8.9
-2.0	11.94	-2.20	11.94	14.14	43	120.4	15.63	13.0	12.5
-1.0	12.70	-1.20	12.70	13.90	44	123.2	18.62	15.1	14.5
0.0	13.41	-0.20	13.41	13.61	46	128.8	21.93	17.0	16.3
1.0	14.07	0.80	14.07	13.27	47	131.6	25.53	19.4	18.5
2.0	14.66	1.80	14.66	12.86	49	137.2	29.24	21.3	20.2
3.0	15.19	2.80	15.19	12.39	50	140.0	33.04	23.6	22.2
4.0	15.64	3.80	15.64	11.84	50	140.0	36.64	26.2	24.5
5.0	16.01	4.80	16.01	11.21	51	142.8	39.90	27.9	25.8
6.0	16.32	5.80	16.32	10.52	51	142.8	42.85	30.0	27.3

Table 17. ARL22M425 power performance at 425 MHz (3.6 V).

425 MHz Package #1		3.6V ; 41 mA							
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(3.6V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-5.62	-20.20	-5.62	14.58	41	147.6	0.27	0.2	0.2
-10.0	4.27	-10.20	4.27	14.47	41	147.6	2.67	1.8	1.7
-8.0	6.46	-8.20	6.46	14.66	42	151.2	4.43	2.9	2.8
-6.0	8.34	-6.20	8.34	14.54	42	151.2	6.82	4.5	4.4
-4.0	10.15	-4.20	10.15	14.35	43	154.8	10.35	6.7	6.4
-2.0	11.82	-2.20	11.82	14.02	44	158.4	15.21	9.6	9.2
-1.0	12.56	-1.20	12.56	13.76	45	162.0	18.03	11.1	10.7
0.0	13.22	-0.20	13.22	13.42	46	165.6	20.99	12.7	12.1
1.0	13.83	0.80	13.83	13.03	47	169.2	24.15	14.3	13.6
2.0	14.41	1.80	14.41	12.61	48	172.8	27.61	16.0	15.1
3.0	14.96	2.80	14.96	12.16	49	176.4	31.33	17.8	16.7
4.0	15.49	3.80	15.49	11.69	50	180.0	35.40	19.7	18.3
5.0	15.97	4.80	15.97	11.17	51	183.6	39.54	21.5	19.9
6.0	16.40	5.80	16.40	10.60	52	187.2	43.65	23.3	21.3

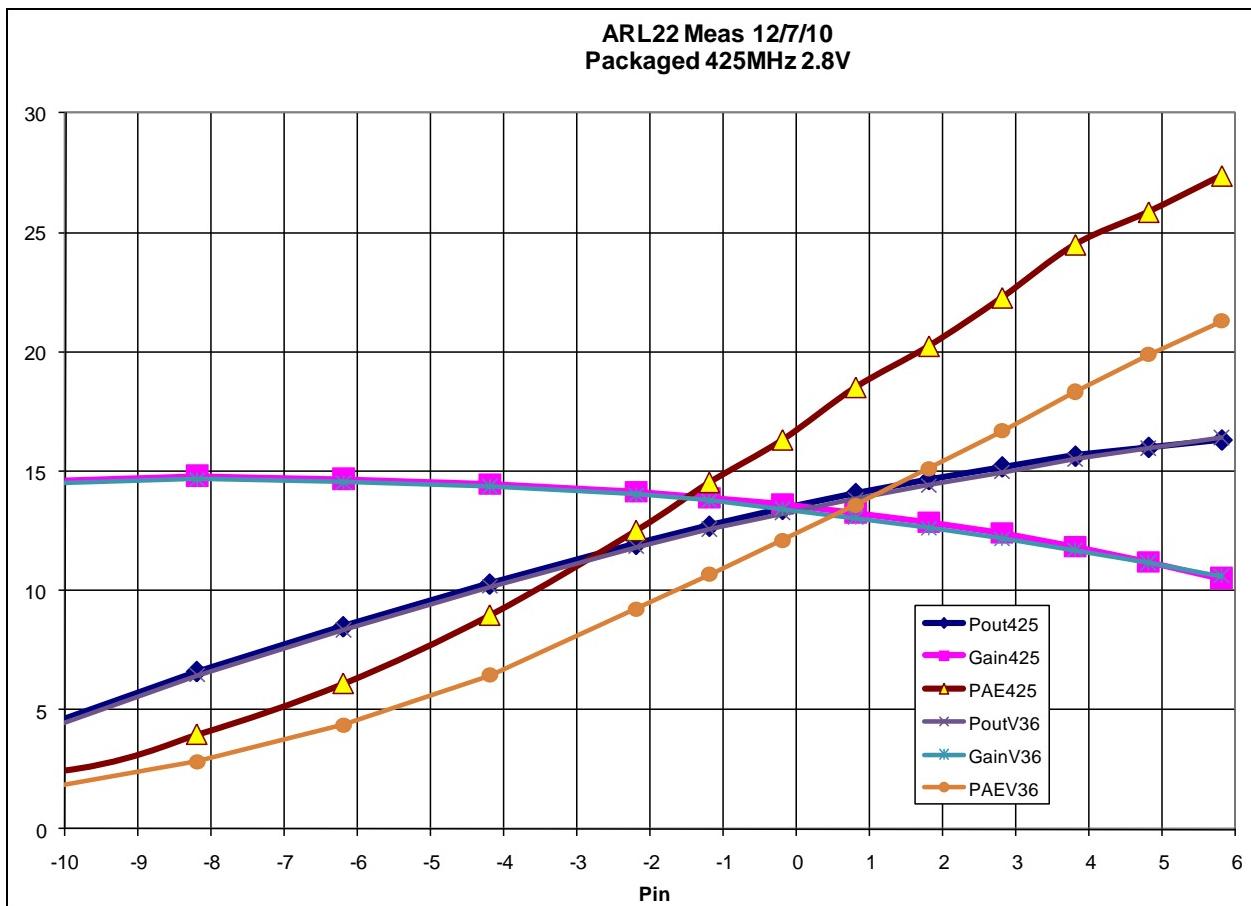


Figure 35. ARL22M425 power performance at 425 MHz (2.8/3.6 V).

Table 18. ARL22M425 power performance at 500 MHz (2.8 V).

12/7/2010 Measured with Power Meter									
500 MHz	Package #1	2.8V ; 39 mA							
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(2.8V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-3.26	-20.20	-3.26	16.94	39	109.2	0.47	0.4	0.4
-10.0	6.65	-10.20	6.65	16.85	39	109.2	4.62	4.2	4.1
-8.0	8.72	-8.20	8.72	16.92	40	112.0	7.45	6.6	6.5
-6.0	10.62	-6.20	10.62	16.82	40	112.0	11.53	10.3	10.1
-4.0	12.48	-4.20	12.48	16.68	40	112.0	17.70	15.8	15.5
-2.0	14.19	-2.20	14.19	16.39	42	117.6	26.24	22.3	21.8
-1.0	14.94	-1.20	14.94	16.14	43	120.4	31.19	25.9	25.3
0.0	15.58	-0.20	15.58	15.78	44	123.2	36.14	29.3	28.6
1.0	16.10	0.80	16.10	15.30	45	126.0	40.74	32.3	31.4
2.0	16.53	1.80	16.53	14.73	46	128.8	44.98	34.9	33.7
3.0	16.87	2.80	16.87	14.07	46	128.8	48.64	37.8	36.3
4.0	17.13	3.80	17.13	13.33	46	128.8	51.64	40.1	38.2
5.0	17.33	4.80	17.33	12.53	46	128.8	54.08	42.0	39.6
6.0	17.48	5.80	17.48	11.68	46	128.8	55.98	43.5	40.5

Table 19. ARL22M425 power performance at 500 MHz (3.6 V).

500 MHz	Package #1						3.6V ; 41 mA		
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(3.6V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-3.42	-20.20	-3.42	16.78	41	147.6	0.45	0.3	0.3
-10.0	6.50	-10.20	6.50	16.70	41	147.6	4.47	3.0	3.0
-8.0	8.58	-8.20	8.58	16.78	41	147.6	7.21	4.9	4.8
-6.0	10.48	-6.20	10.48	16.68	41	147.6	11.17	7.6	7.4
-4.0	12.34	-4.20	12.34	16.54	42	151.2	17.14	11.3	11.1
-2.0	14.08	-2.20	14.08	16.28	43	154.8	25.59	16.5	16.1
-1.0	14.88	-1.20	14.88	16.08	44	158.4	30.76	19.4	18.9
0.0	15.59	-0.20	15.59	15.79	45	162.0	36.22	22.4	21.8
1.0	16.23	0.80	16.23	15.43	46	165.6	41.98	25.3	24.6
2.0	16.80	1.80	16.80	15.00	47	169.2	47.86	28.3	27.4
3.0	17.29	2.80	17.29	14.49	49	176.4	53.58	30.4	29.3
4.0	17.70	3.80	17.70	13.90	49	176.4	58.88	33.4	32.0
5.0	18.04	4.80	18.04	13.24	50	180.0	63.68	35.4	33.7
6.0	18.31	5.80	18.31	12.51	50	180.0	67.76	37.6	35.5

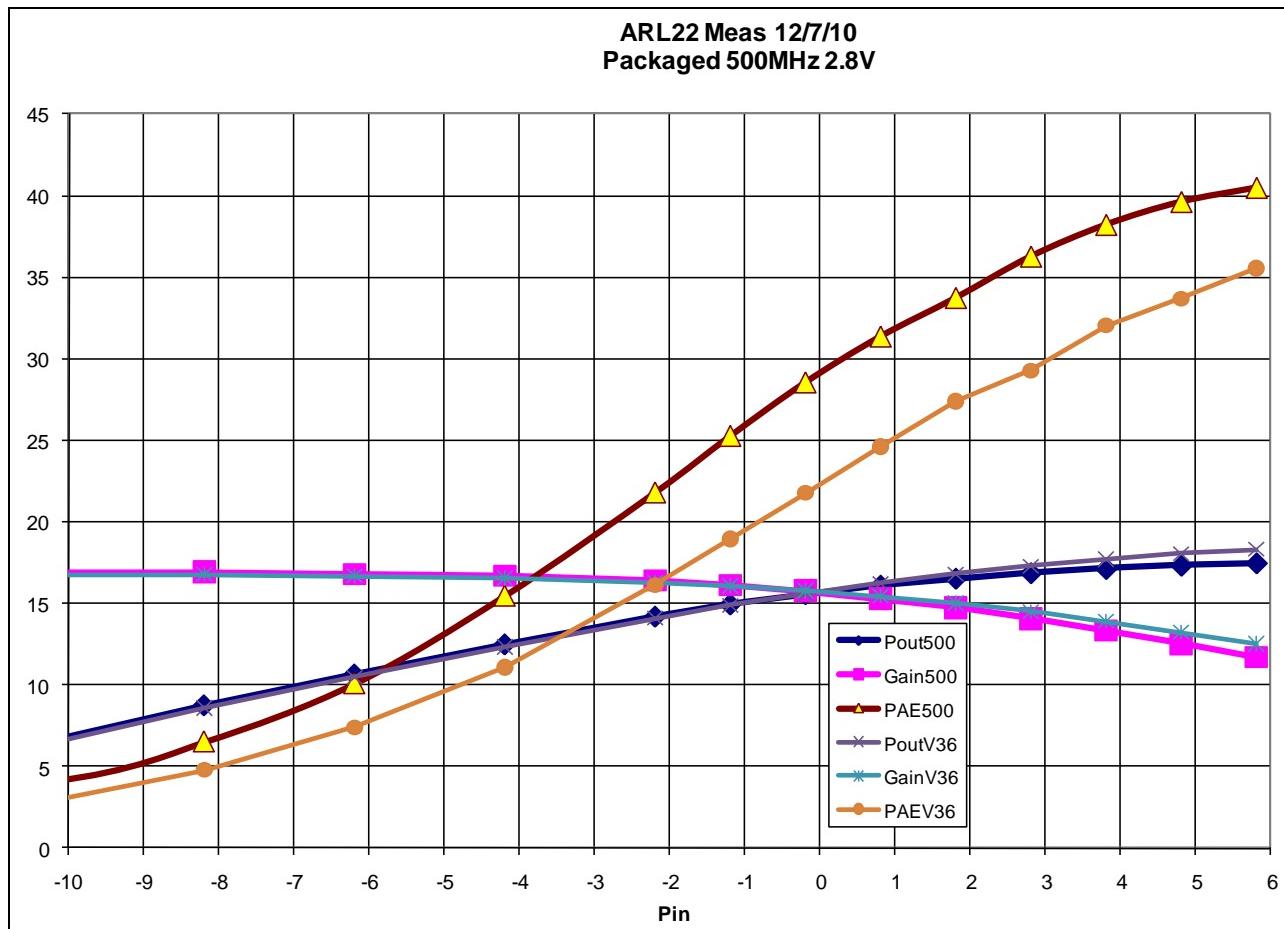


Figure 36. ARL22M425 power performance at 500 MHz (2.8/3.6 V).

Table 20. ARL22M425 power performance at 600 MHz (2.8 V).

12/7/2010 Measured with Power Meter									
600 MHz	Package #1		2.8V ; 39 mA						
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(2.8V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-3.12	-20.20	-3.12	17.08	39	109.2	0.49	0.4	0.4
-10.0	6.83	-10.20	6.83	17.03	39	109.2	4.82	4.4	4.3
-8.0	8.84	-8.20	8.84	17.04	39	109.2	7.66	7.0	6.9
-6.0	10.79	-6.20	10.79	16.99	39	109.2	11.99	11.0	10.8
-4.0	12.72	-4.20	12.72	16.92	40	112.0	18.71	16.7	16.4
-2.0	14.53	-2.20	14.53	16.73	40	112.0	28.38	25.3	24.8
-1.0	15.34	-1.20	15.34	16.54	41	114.8	34.20	29.8	29.1
0.0	16.02	-0.20	16.02	16.22	41	114.8	39.99	34.8	34.0
1.0	16.55	0.80	16.55	15.75	42	117.6	45.19	38.4	37.4
2.0	16.96	1.80	16.96	15.16	43	120.4	49.66	41.2	40.0
3.0	17.27	2.80	17.27	14.47	43	120.4	53.33	44.3	42.7
4.0	17.50	3.80	17.50	13.70	43	120.4	56.23	46.7	44.7
5.0	17.65	4.80	17.65	12.85	43	120.4	58.21	48.3	45.8
6.0	17.76	5.80	17.76	11.96	42	117.6	59.70	50.8	47.5

Table 21. ARL22M425 power performance at 600 MHz (3.6 V).

600 MHz	Package #1		3.6V ; 41 mA						
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(3.6V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-3.21	-20.20	-3.21	16.99	41	147.6	0.48	0.3	0.3
-10.0	6.73	-10.20	6.73	16.93	41	147.6	4.71	3.2	3.1
-8.0	8.74	-8.20	8.74	16.94	41	147.6	7.48	5.1	5.0
-6.0	10.68	-6.20	10.68	16.88	41	147.6	11.69	7.9	7.8
-4.0	12.60	-4.20	12.60	16.80	41	147.6	18.20	12.3	12.1
-2.0	14.47	-2.20	14.47	16.67	42	151.2	27.99	18.5	18.1
-1.0	15.35	-1.20	15.35	16.55	42	151.2	34.28	22.7	22.2
0.0	16.17	-0.20	16.17	16.37	43	154.8	41.40	26.7	26.1
1.0	16.89	0.80	16.89	16.09	44	158.4	48.87	30.8	30.1
2.0	17.52	1.80	17.52	15.72	45	162.0	56.49	34.9	33.9
3.0	18.03	2.80	18.03	15.23	46	165.6	63.53	38.4	37.2
4.0	18.43	3.80	18.43	14.63	47	169.2	69.66	41.2	39.8
5.0	18.73	4.80	18.73	13.93	47	169.2	74.64	44.1	42.3
6.0	18.94	5.80	18.94	13.14	48	172.8	78.34	45.3	43.1

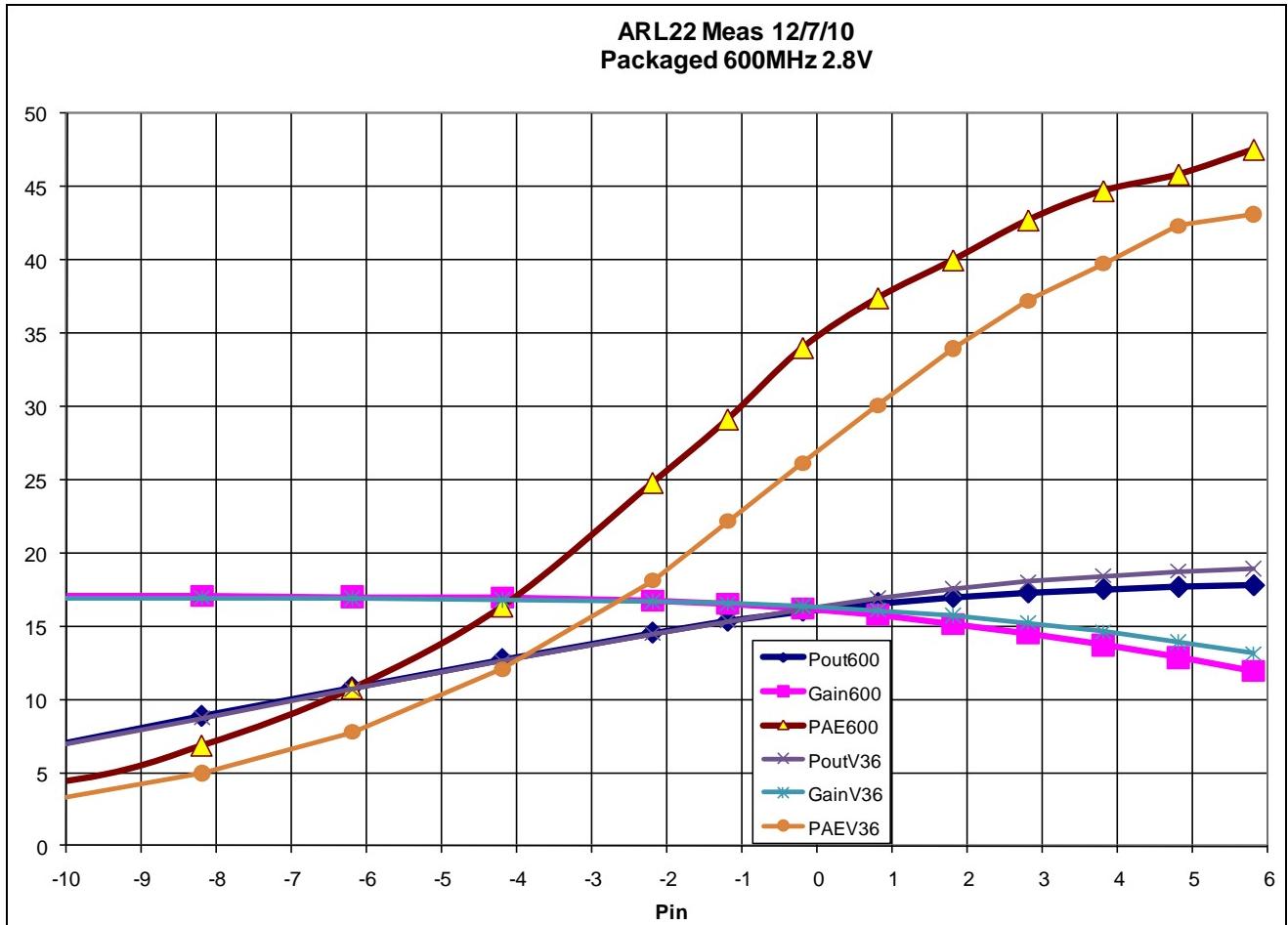


Figure 37. ARL22M425 power performance at 600 MHz (2.8/3.6 V).

ARL23M425 RFIC: This 425 MHz Booster IC design consists of a TR Switch, a BPSK modulator, a broadband power amplifier based on the 1st pass designs, and a low current low noise amplifier (figure 38). S-parameter measurements were made of the transmit and receive modes, as well as performance measurements. Isolation from the TR switch was measured with the TR switch in receive mode while measuring the transmit isolation, similarly for the transmit mode isolation. There was little change in performance at 2.8 V versus 3.6 V, as the designs are intended to be robust over a battery supply range of about 2 V up to 5 V (even 6 V or higher is possible with reduced efficiency). The broadband power amplifier re-used from the 1st pass designs worked well. The power amplifier had good efficiency at 2.8 V and 3.6 V.

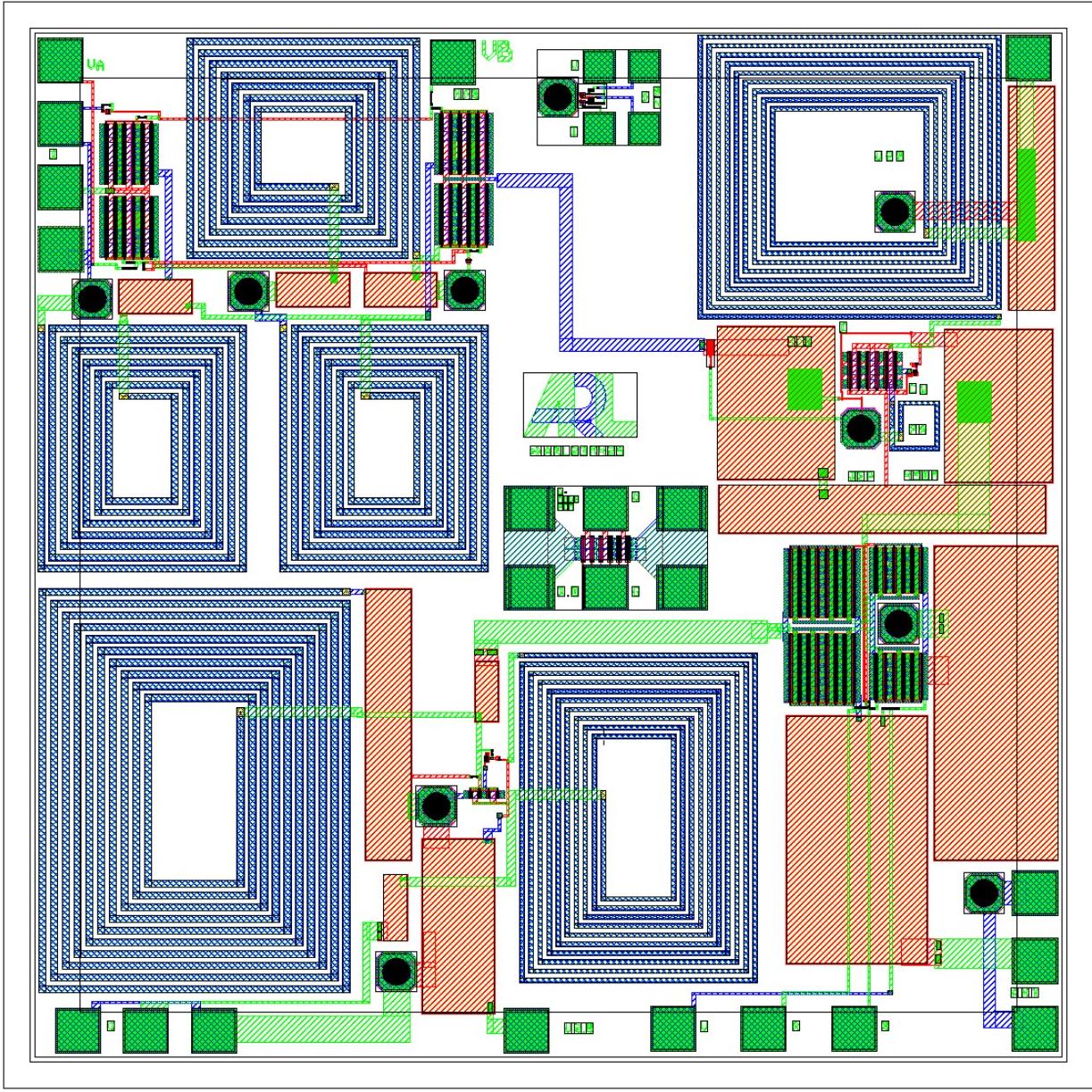


Figure 38. Plot of ARL23M425 test chip (BPSK, broadband PA, broadband LNA, & TRS).

Figure 39 shows just about 15.5 dB gain for the high pass and low pass states of the BPSK modulator with about 43 dB of isolation for the transmit path when switched to receive. Figure 40 shows the relative phase shift between the two BPSK states—which is very close to the ideal 180 degrees at 400 MHz. Input return loss (figure 41) is only about 8 dB for the transmit state, even when in the isolation/receive mode. Output return loss (figure 42) is a good 17 dB for the transmit state, and is a little worse in the isolation/receive mode.

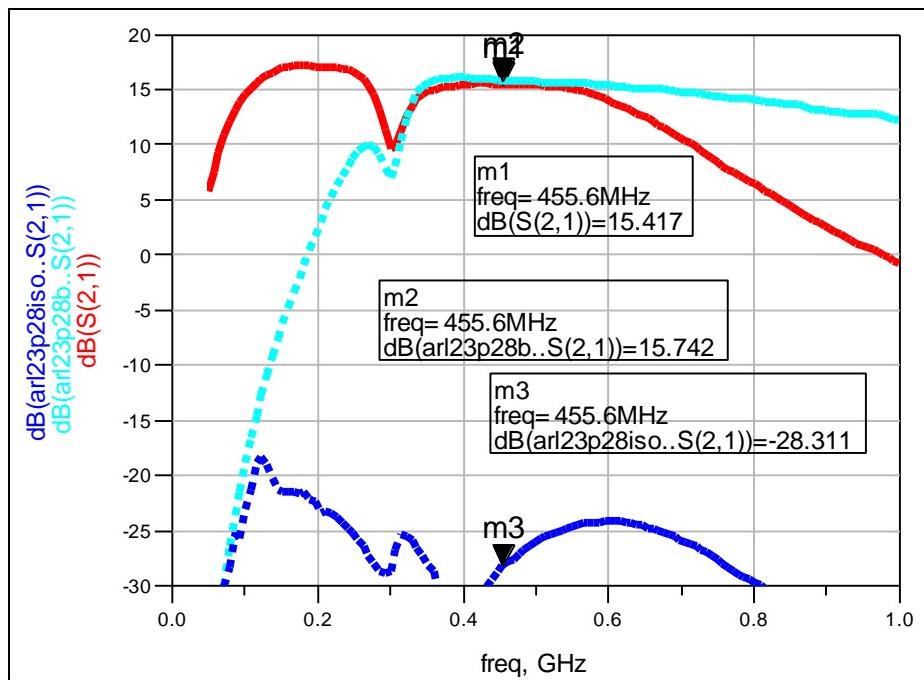


Figure 39. Transmit gain/isolation S21 in package (ARL23M425 at 2.8 V).

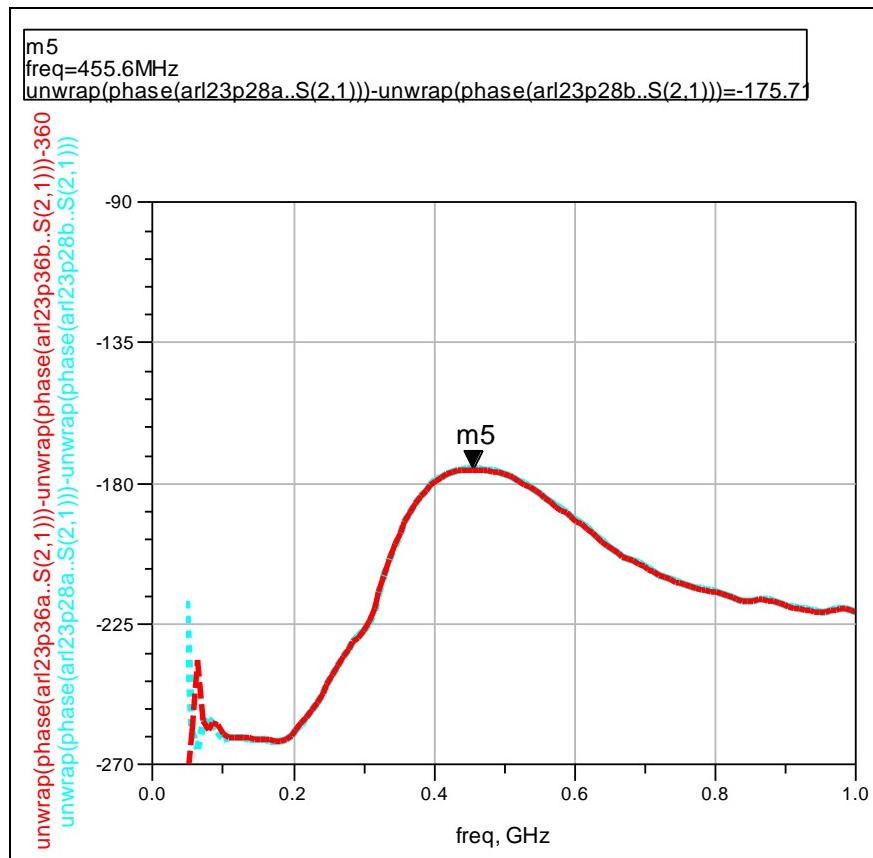


Figure 40. Relative BPSK transmit phase S21 in package (ARL23M425 at 2.8/3.6 V).

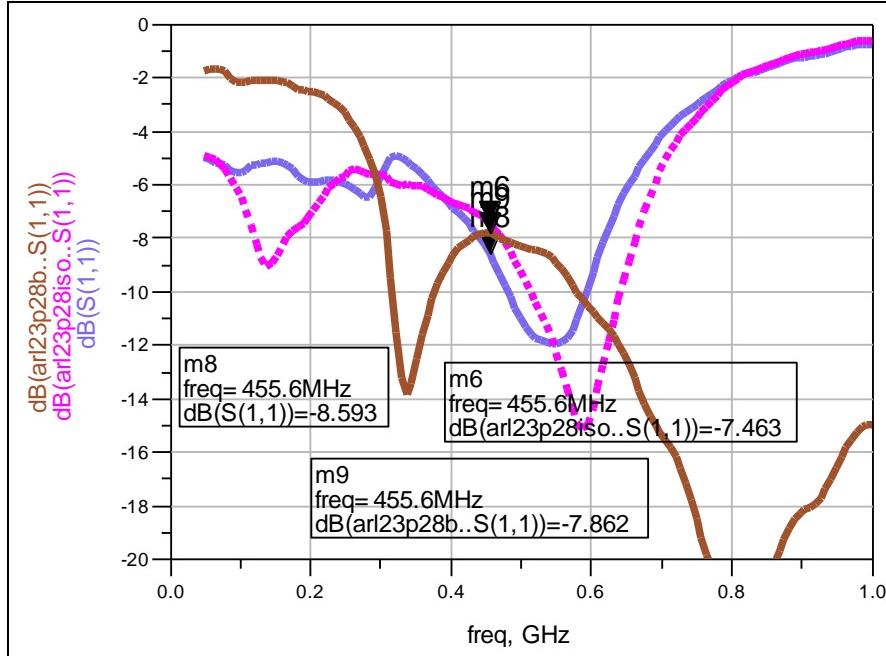


Figure 41. Transmit input return loss S11 in package (ARL23M425 at 2.8 V).

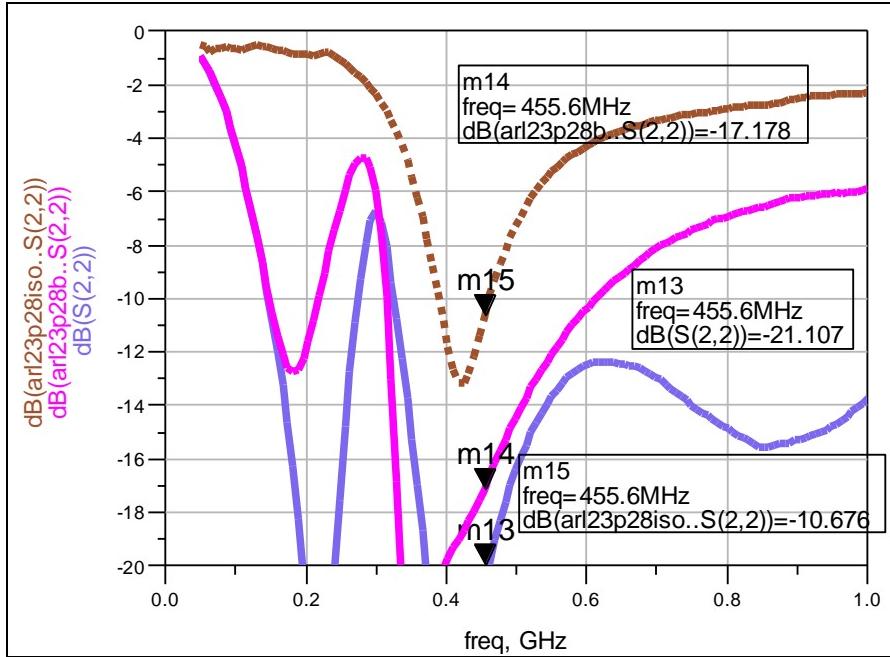


Figure 42. Transmit output return loss S22 in package (ARL23M425 at 2.8 V).

For the receive state, figure 43 shows just over 10 dB gain for the low noise amplifier and TR switch loss, with about 42 dB of isolation for the receive path when switched to transmit. Input return loss (figure 44) is a decent 10 dB for the receive state, but is worse when in the isolation/transmit mode. Output return loss (figure 45) is very good at 17 dB for the receive state, and is about the same in the isolation/transmit mode.

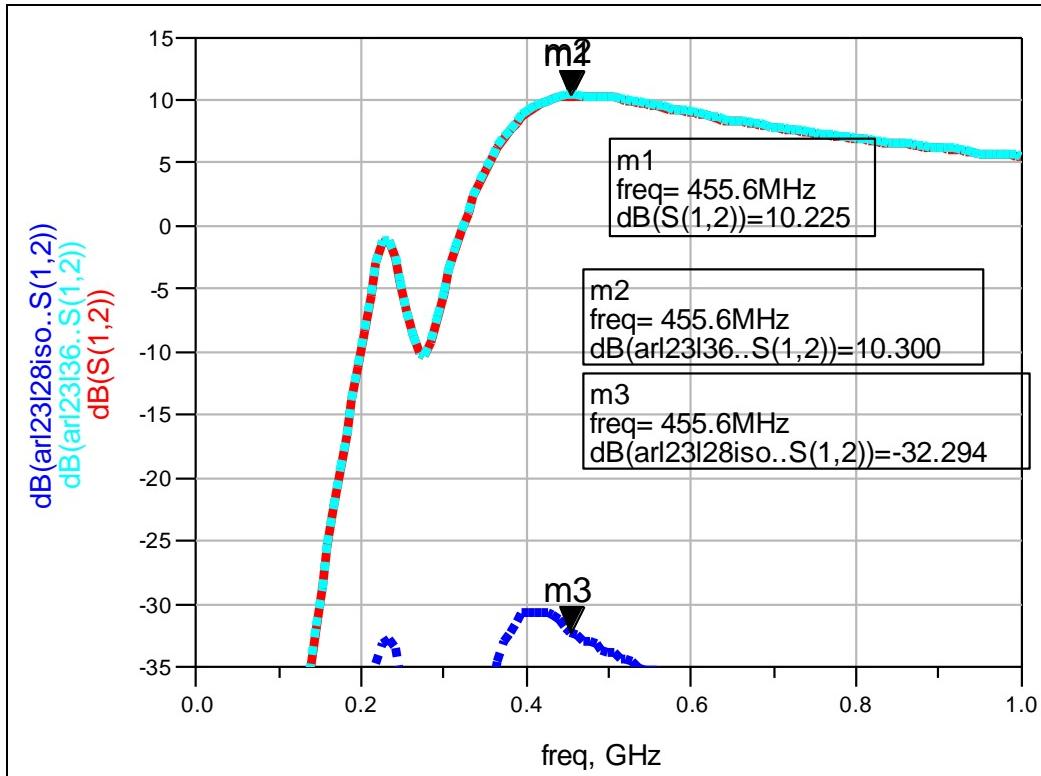


Figure 43. Transmit gain/isolation S21 in package (ARL23M425 at 2.8 V).

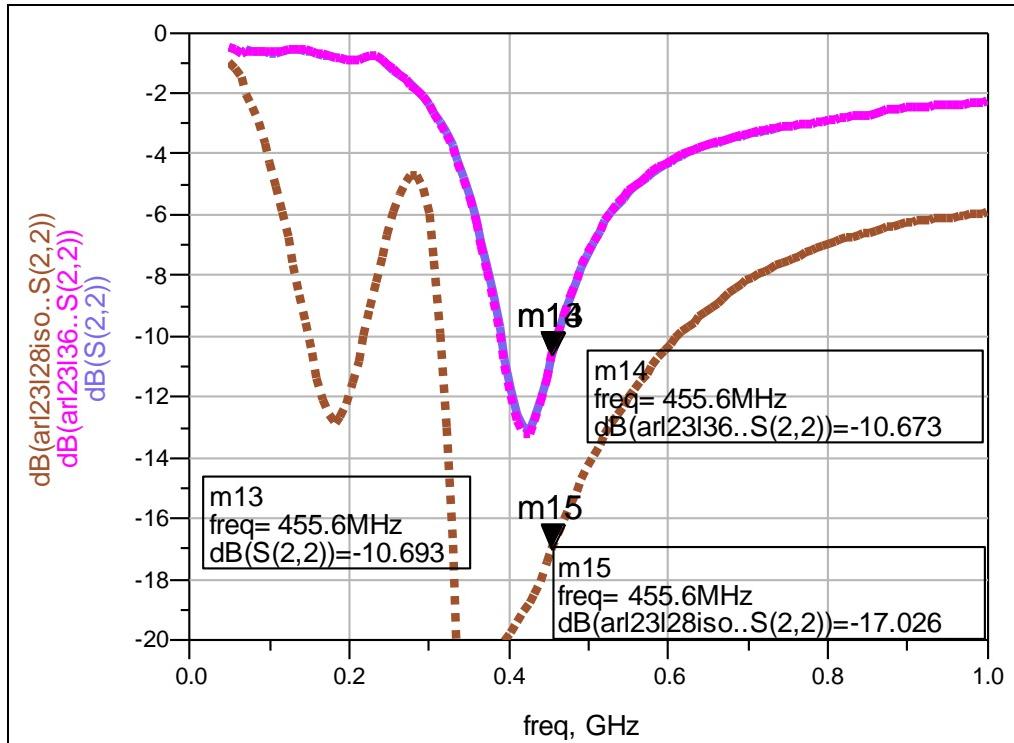


Figure 44. Receive input return loss in package (ARL23M425 at 2.8 V).

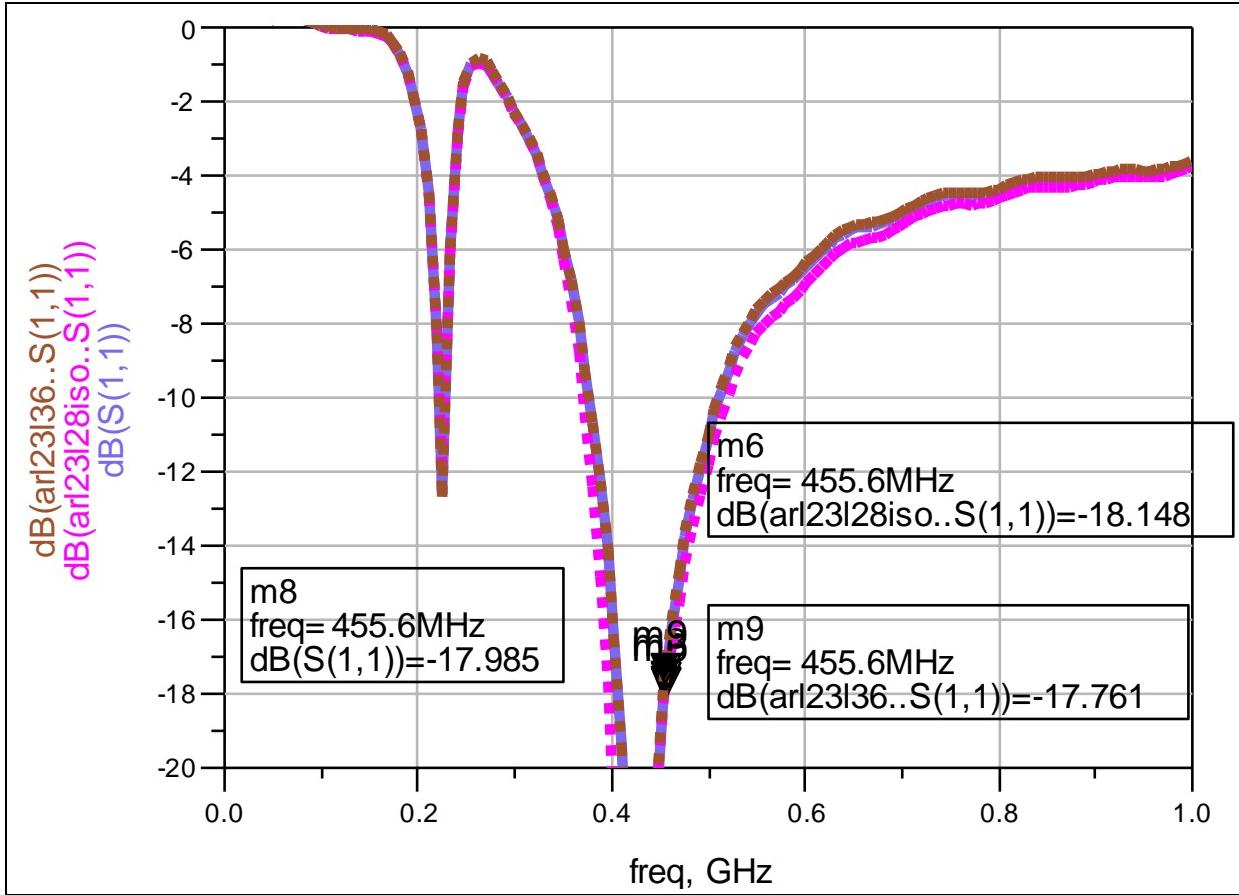


Figure 45. Receive output return loss in package (ARL23M425 at 2.8 V).

ARL23M425 Performance: While switched to the transmit path, I measured the RF output power of the packaged Booster IC versus the input power to yield power added efficiency, gain, and DC power consumption. These measurements were performed at 2.8 V and 3.6 V, presuming a regulated power supply from either a 3.0 V battery or a 3.9 V lithium battery, at 425 MHz. Table 22 shows the measured performance at 2.8 V and 425 MHz, while table 23 is at 3.6 V. Figure 46, shows a plot summarizing the measurements versus RF input Power. At 3 dB compression and 425 MHz, the power added efficiency is about 36% and increases a bit at higher compression levels, i.e., higher RF input levels. At 425 MHz and 2.8 V, the output power is only 30 mW, but is about 44 mW at 3.6 V, with slightly worse efficiency at 34%.

Table 22. ARL23M425 power performance at 425 MHz (2.8 V).

12/7/2010 Measured with Power Meter									
425 MHz	Package #1		2.8V ; 42 mA						
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(2.8V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-4.88	-20.20	-4.88	15.32	42	117.6	0.33	0.3	0.3
-10.0	5.05	-10.20	5.05	15.25	41	114.8	3.20	2.8	2.7
-8.0	7.29	-8.20	7.29	15.49	41	114.8	5.36	4.7	4.5
-6.0	9.24	-6.20	9.24	15.44	40	112.0	8.39	7.5	7.3
-4.0	11.11	-4.20	11.11	15.31	40	112.0	12.91	11.5	11.2
-2.0	12.83	-2.20	12.83	15.03	37	103.6	19.19	18.5	17.9
-1.0	13.55	-1.20	13.55	14.75	35	98.0	22.65	23.1	22.3
0.0	14.11	-0.20	14.11	14.31	34	95.2	25.76	27.1	26.1
1.0	14.48	0.80	14.48	13.68	32	89.6	28.05	31.3	30.0
2.0	14.72	1.80	14.72	12.92	31	86.8	29.65	34.2	32.4
3.0	14.87	2.80	14.87	12.07	30	84.0	30.69	36.5	34.3
4.0	14.97	3.80	14.97	11.17	29	81.2	31.41	38.7	35.7

Table 23. ARL23M425 power performance at 425 MHz (3.6 V).

425 MHz Package #1									
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(3.6V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-4.87	-20.20	-4.87	15.33	44	158.4	0.33	0.2	0.2
-10.0	5.07	-10.20	5.07	15.27	43	154.8	3.21	2.1	2.0
-8.0	7.30	-8.20	7.30	15.50	43	154.8	5.37	3.5	3.4
-6.0	9.26	-6.20	9.26	15.46	43	154.8	8.43	5.4	5.3
-4.0	11.19	-4.20	11.19	15.39	42	151.2	13.15	8.7	8.4
-2.0	13.05	-2.20	13.05	15.25	42	151.2	20.18	13.3	13.0
-1.0	13.95	-1.20	13.95	15.15	41	147.6	24.83	16.8	16.3
0.0	14.77	-0.20	14.77	14.97	40	144.0	29.99	20.8	20.2
1.0	15.42	0.80	15.42	14.62	40	144.0	34.83	24.2	23.4
2.0	15.87	1.80	15.87	14.07	38	136.8	38.64	28.2	27.1
3.0	16.16	2.80	16.16	13.36	37	133.2	41.30	31.0	29.6
4.0	16.36	3.80	16.36	12.56	36	129.6	43.25	33.4	31.5
5.0	16.53	4.80	16.53	11.73	35	126.0	44.98	35.7	33.3

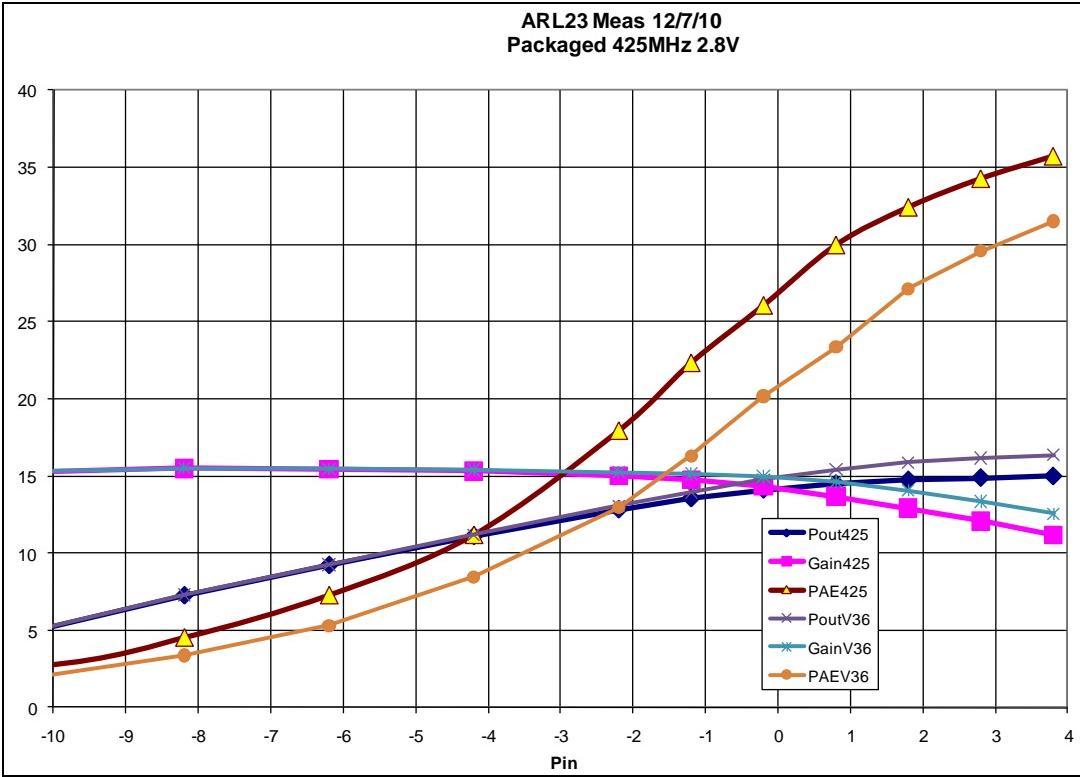


Figure 46. ARL23M425 power performance at 425 MHz (2.8/3.6 V).

On the receive side, the noise figure and gain were measured at 450 MHz to be 10.6 dB and 4.1 dB, respectively. The gain was about as expected but the noise figure was higher than that predicted by simulations, and is considerably higher than the identical receive configuration for ARL21M425. I am not sure why the same amplifier had a higher noise figure measurement in ARL22M425 and ARL23M425.

ARL24DB RFIC: This dual band 400 to 950 MHz Booster IC design consists of a TR Switch, a dual band BPSK modulator, a broadband power amplifier based on the 1st pass designs, and a broadband low noise amplifier based on the 1st pass designs (figure 47). S-parameter measurements were made of the transmit and receive modes as well as performance measurements. Isolation from the TR switch was measured with the TR switch in receive mode, while measuring the transmit isolation and similarly for the transmit mode isolation. There was little change in performance at 2.8 V versus 3.6 V, as the designs are intended to be robust over a battery supply range of just over 2 V up to 5 V (even 6 V or higher is possible with less efficiency). The BPSK modulator was broad banded by using more elements to achieve 180 degree relative phase difference at 425 MHz and 900 MHz. Since the power amplifier from the 1st pass designs worked well and was broadband, it was used for this Booster IC. The power amplifier had good efficiency at 2.8 V and 3.6 V. A tweak of the current consumption for the broadband low noise amplifier based on the 1st pass design, reduced its current consumption from about 17 mA to 9 mA while retaining good gain.

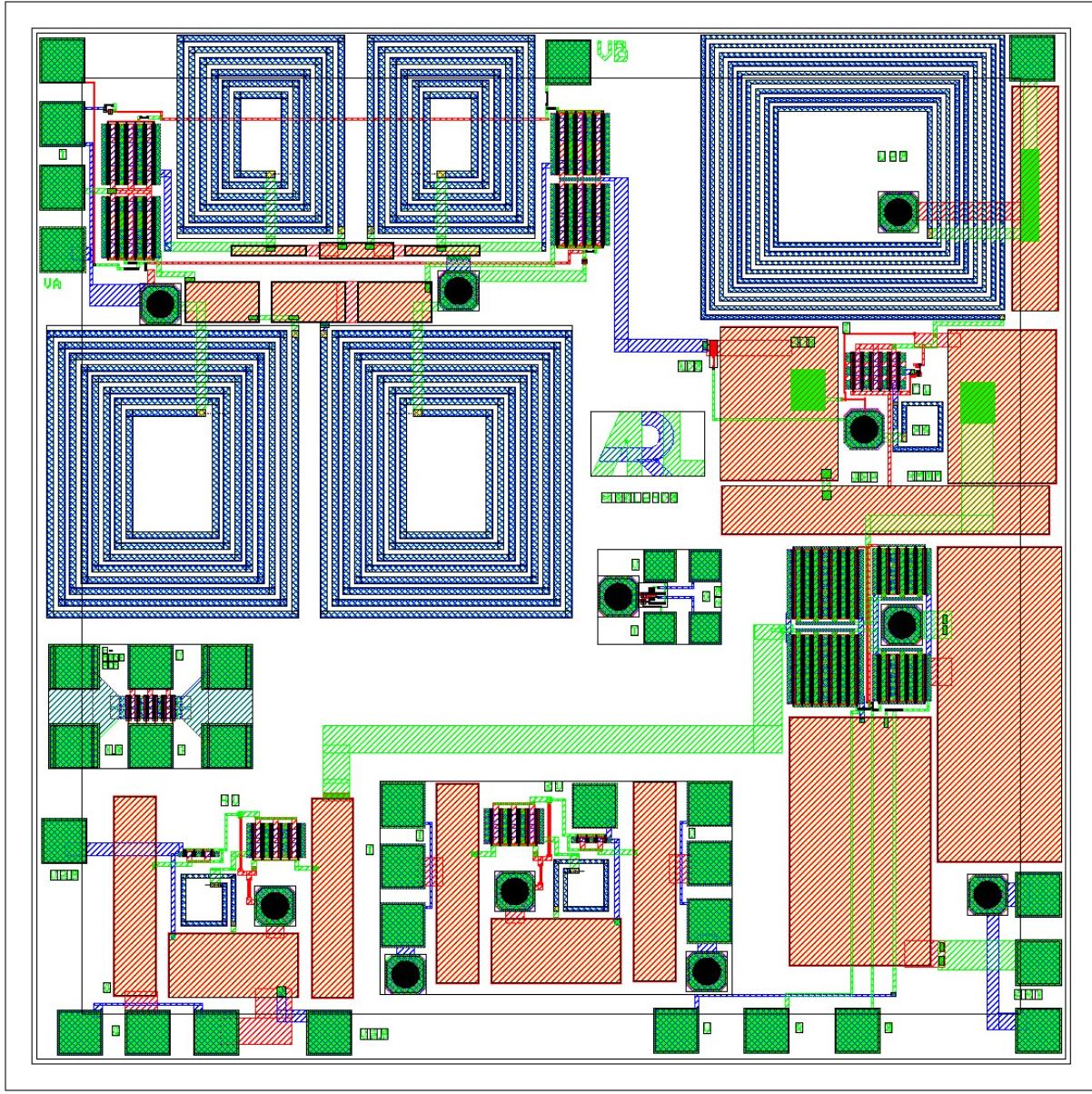


Figure 47. Plot of ARL24DB test chip (broadband BPSK, PA, LNA, & TRS).

Figure 48 shows just about 15.1 dB gain for the high pass and low pass states of the BPSK modulator with about 42 dB of isolation for the transmit path when switched to receive. Figure 49 shows the relative phase shift between the two BPSK states—which is very close to the ideal 180 degrees at 425 MHz and again at 950 MHz. Input return loss (figure 50) is only about 8 dB for the transmit state, even when in the isolation/receive mode. Output return loss (figure 51) is an excellent 19 dB for the transmit state, and is a little worse in the isolation/receive mode.

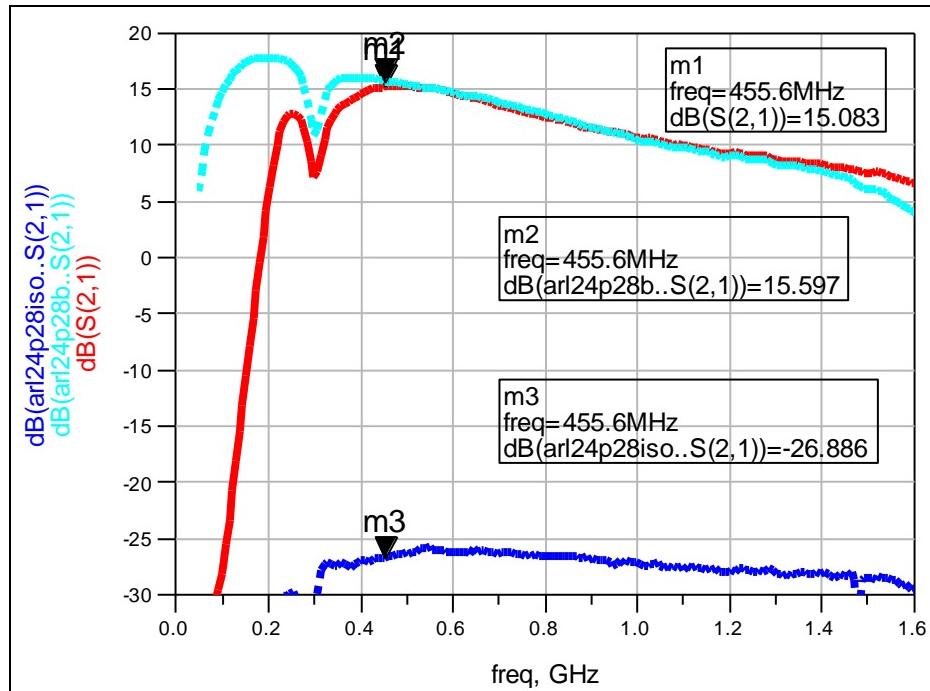


Figure 48. Transmit gain/isolation S21 in package (ARL24DB at 2.8 V).

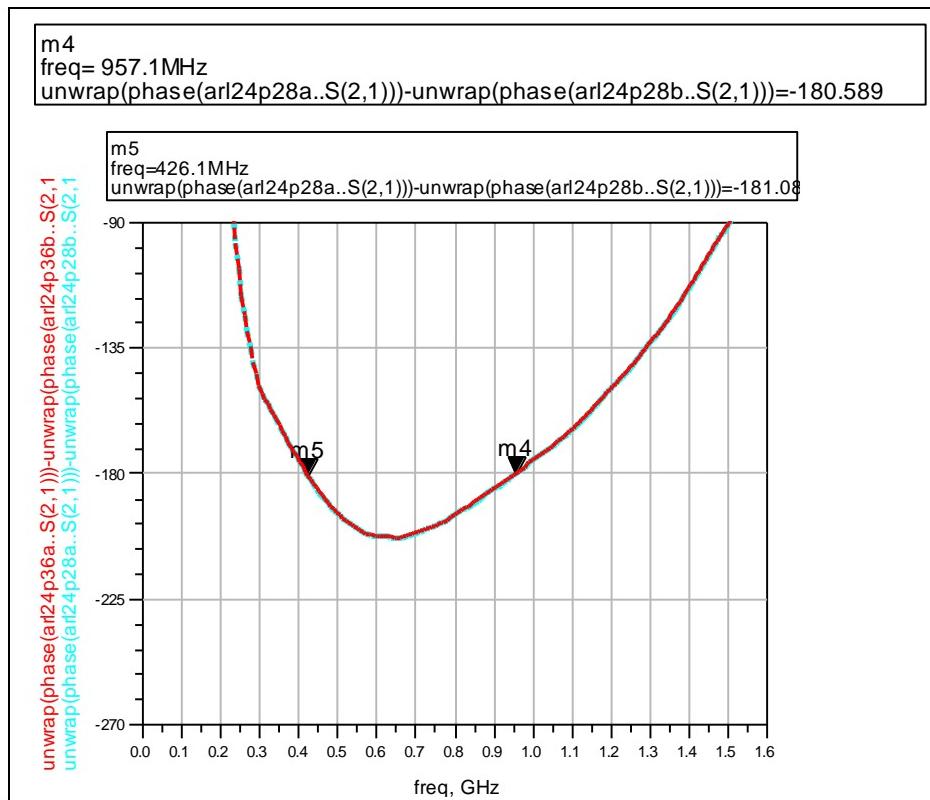


Figure 49. Relative BPSK transmit phase S21 in package (ARL24DB at 2.8/3.6 V).

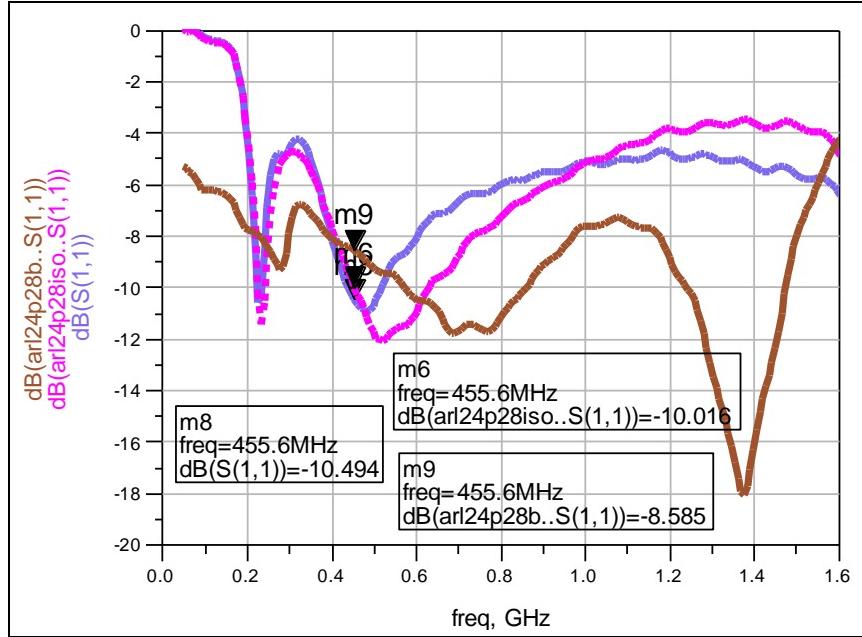


Figure 50. Transmit input return loss S11 in package (2.8 V).

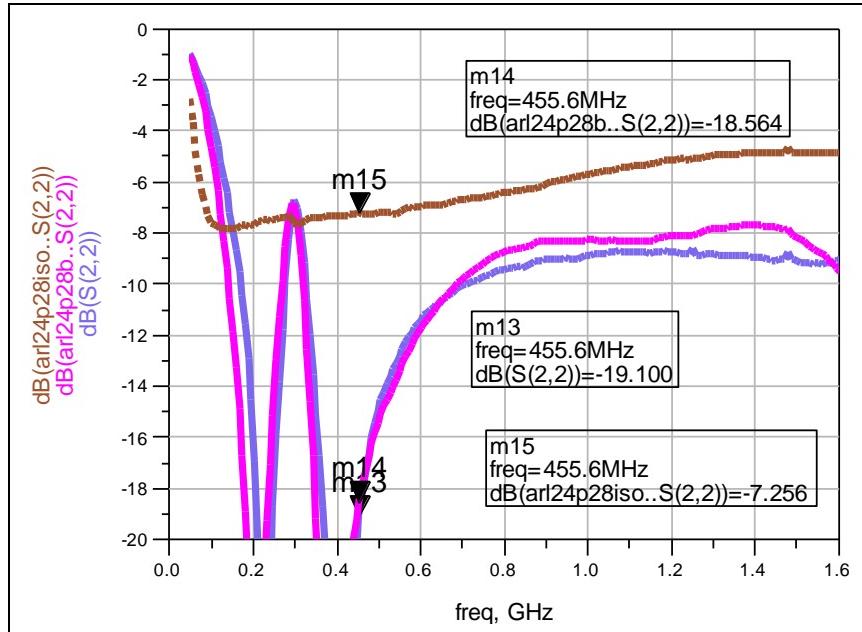


Figure 51. Transmit output return loss S22 in package (ARL24DB at 2.8 V).

For the receive state, figure 52 shows just over 14 dB gain for the low noise amplifier and TR switch loss, with about 44 dB of isolation for the receive path when switched to transmit. Input return loss (figure 53) is a OK 8 dB for the receive state, but is worse when in the isolation/transmit mode. Output return loss (figure 54) is only 7 dB for the receive state, and is a little better in the isolation/transmit mode.

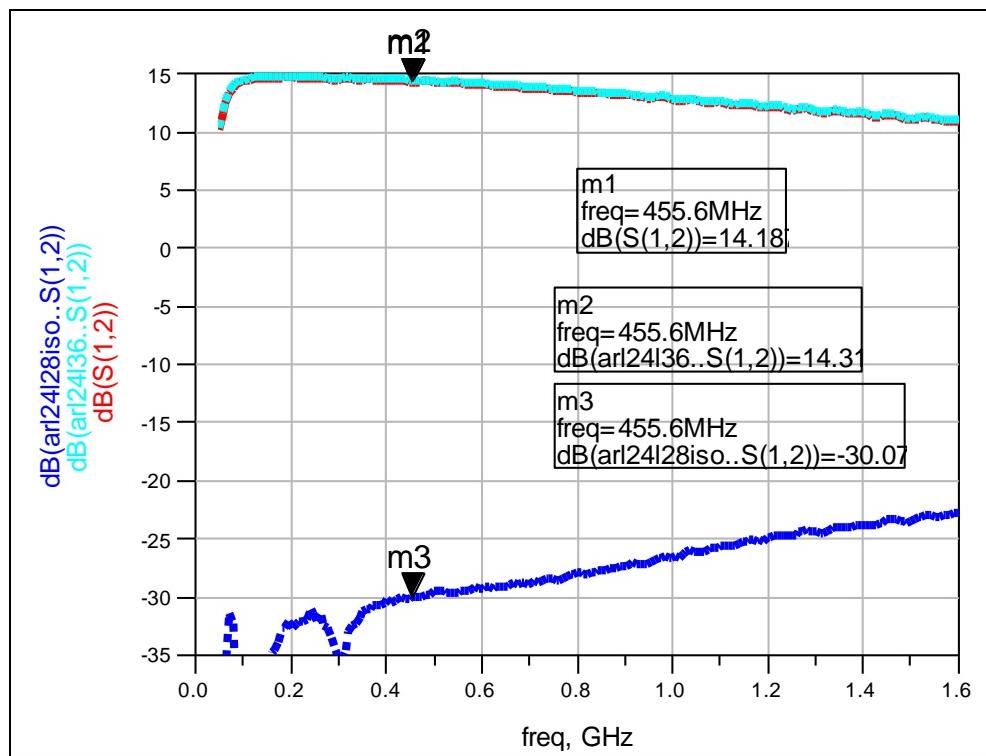


Figure 52. Transmit gain/isolation S21 in package (ARL24DB at 2.8 V).

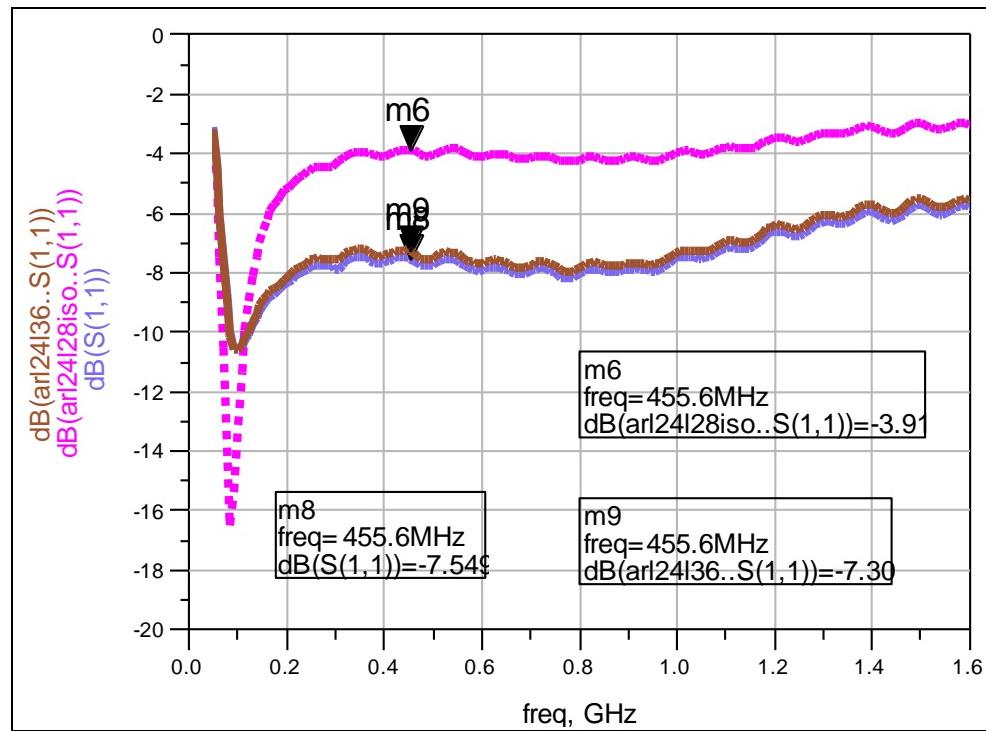


Figure 53. Receive input return loss in package (ARL24DB at 2.8 V).

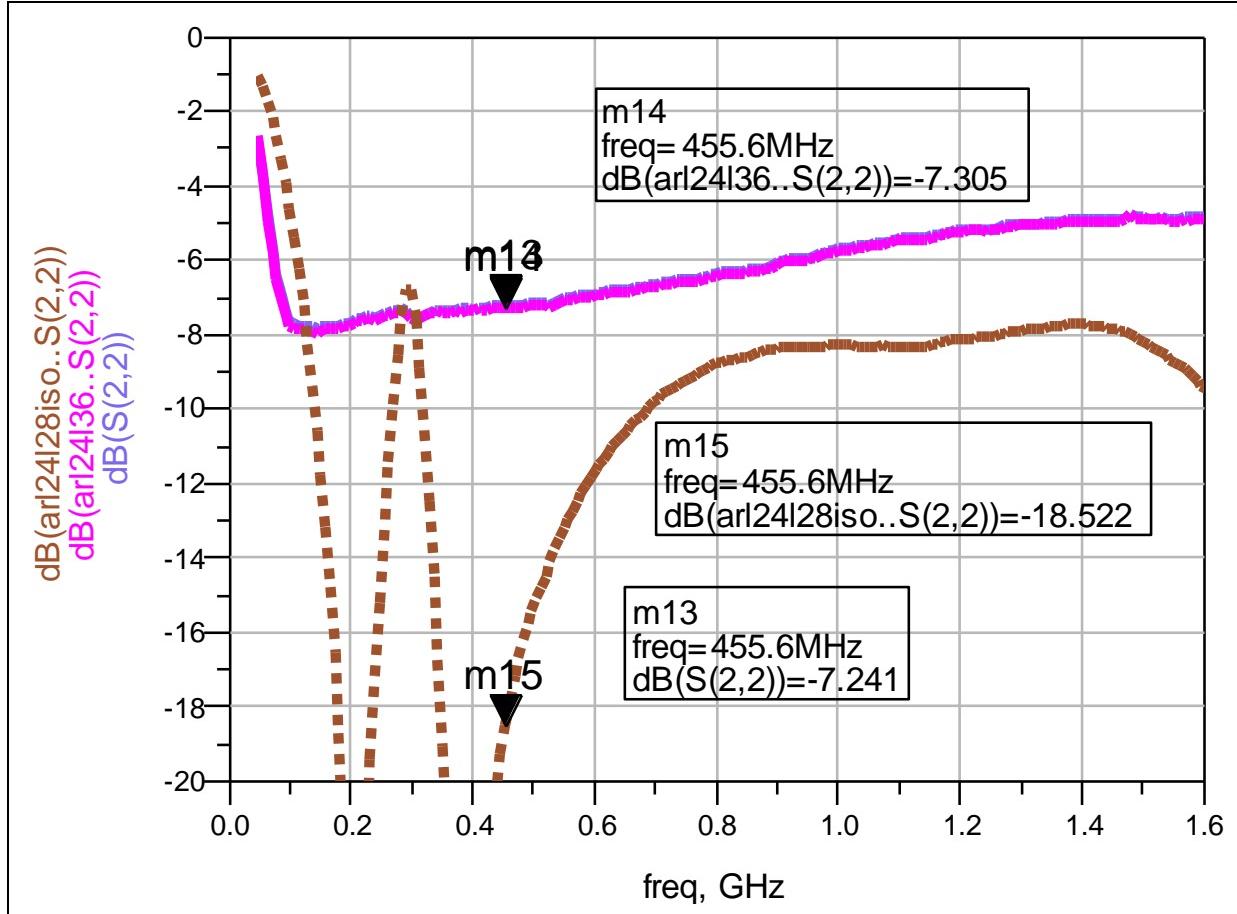


Figure 54. Receive output return loss in package (ARL24DB at 2.8 V).

ARL24DB Performance: While switched to the transmit path, I measured the RF output power of the packaged Booster IC versus the input power to yield power added efficiency, gain, and DC power consumption. These measurements were performed at 2.8 V and 3.6 V, presuming a regulated power supply from either a 3.0 V battery or a 3.9 V lithium battery, at 425 MHz and 900 MHz. Table 24 shows the measured performance at 2.8 V and 425 MHz, while table 25 is at 3.6 V. Figure 55, shows a plot summarizing the measurements versus RF input Power. Tables 26 and 27, plus figure 56 show the measured performance at 900 MHz. At 3 dB compression and 425 MHz, the power added efficiency is about 35% and increases a bit at higher compression levels, i.e., higher RF input levels. At 425 MHz and 2.8 V, the output power is only 30 mW, but is over 42 mW at 3.6V, with more than 31% PAE.

Table 24. ARL24DB power performance at 425 MHz (2.8 V).

425 MHz	Package #1						2.8V ; 40 mA		
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(2.8V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-5.52	-20.20	-5.52	14.68	40	112.0	0.28	0.3	0.2
-10.0	4.49	-10.20	4.49	14.69	40	112.0	2.81	2.5	2.4
-8.0	6.77	-8.20	6.77	14.97	40	112.0	4.75	4.2	4.1
-6.0	8.77	-6.20	8.77	14.97	39	109.2	7.53	6.9	6.7
-4.0	10.72	-4.20	10.72	14.92	39	109.2	11.80	10.8	10.5
-2.0	12.56	-2.20	12.56	14.76	38	106.4	18.03	16.9	16.4
-1.0	13.35	-1.20	13.35	14.55	36	100.8	21.63	21.5	20.7
0.0	13.97	-0.20	13.97	14.17	35	98.0	24.95	25.5	24.5
1.0	14.38	0.80	14.38	13.58	34	95.2	27.42	28.8	27.5
2.0	14.63	1.80	14.63	12.83	33	92.4	29.04	31.4	29.8
3.0	14.82	2.80	14.82	12.02	32	89.6	30.34	33.9	31.7
4.0	14.96	3.80	14.96	11.16	31	86.8	31.33	36.1	33.3

Table 25. ARL24DB power performance at 425 MHz (3.6 V).

425 MHz	Package #1						3.6V ; 43 mA		
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(3.6V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-5.51	-20.20	-5.51	14.69	43	154.8	0.28	0.2	0.2
-10.0	4.50	-10.20	4.50	14.70	42	151.2	2.82	1.9	1.8
-8.0	6.78	-8.20	6.78	14.98	42	151.2	4.76	3.2	3.1
-6.0	8.77	-6.20	8.77	14.97	42	151.2	7.53	5.0	4.8
-4.0	10.74	-4.20	10.74	14.94	41	147.6	11.86	8.0	7.8
-2.0	12.66	-2.20	12.66	14.86	41	147.6	18.45	12.5	12.1
-1.0	13.59	-1.20	13.59	14.79	40	144.0	22.86	15.9	15.3
0.0	14.43	-0.20	14.43	14.63	40	144.0	27.73	19.3	18.6
1.0	15.13	0.80	15.13	14.33	39	140.4	32.58	23.2	22.4
2.0	15.62	1.80	15.62	13.82	39	140.4	36.48	26.0	24.9
3.0	15.96	2.80	15.96	13.16	38	136.8	39.45	28.8	27.4
4.0	16.21	3.80	16.21	12.41	37	133.2	41.78	31.4	29.6

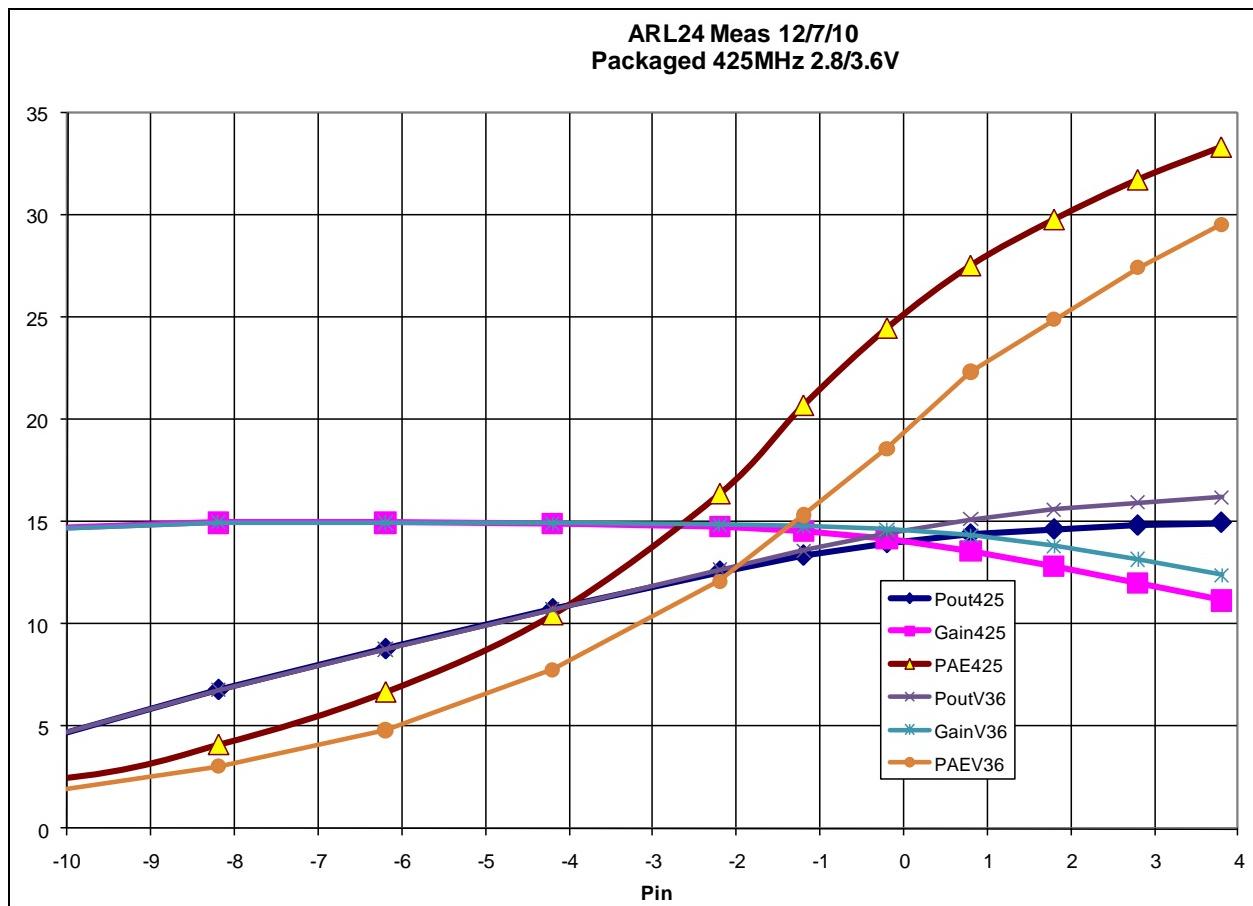


Figure 55. ARL24DB power performance at 425 MHz (2.8/3.6 V).

Table 26. ARL24DB power performance at 900 MHz (2.8 V).

12/7/2010 Measured with Power Meter									
900 MHz	Package #1			2.8V ; 40 mA					
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(2.8V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-1.33	-20.40	-8.79	11.61	40	112.0	0.13	0.1	0.1
-10.0	8.66	-10.40	1.21	11.61	40	112.0	1.32	1.2	1.1
-8.0	10.76	-8.40	3.56	11.96	40	112.0	2.27	2.0	1.9
-6.0	12.75	-6.40	5.56	11.96	40	112.0	3.60	3.2	3.0
-4.0	14.68	-4.40	7.55	11.95	40	112.0	5.69	5.1	4.8
-2.0	16.36	-2.40	9.52	11.92	39	109.2	8.95	8.2	7.7
-1.0	17.63	-1.40	10.51	11.91	39	109.2	11.25	10.3	9.6
0.0	18.10	-0.40	11.47	11.87	39	109.2	14.03	12.8	12.0
1.0	18.46	0.60	12.40	11.80	38	106.4	17.38	16.3	15.3
2.0	18.73	1.60	13.25	11.65	37	103.6	21.13	20.4	19.0
3.0	18.92	2.60	13.94	11.34	36	100.8	24.77	24.6	22.8
4.0	19.03	3.60	14.33	10.73	35	98.0	27.10	27.7	25.3

Table 27. ARL24DB power performance at 900 MHz (3.6 V).

900 MHz	Package #1						3.6V ; 43 mA		
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(3.6V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-8.79	-20.40	-8.79	11.61	43	154.8	0.13	0.1	0.1
-10.0	1.21	-10.40	1.21	11.61	42	151.2	1.32	0.9	0.8
-8.0	3.56	-8.40	3.56	11.96	42	151.2	2.27	1.5	1.4
-6.0	5.56	-6.40	5.56	11.96	42	151.2	3.60	2.4	2.2
-4.0	7.55	-4.40	7.55	11.95	42	151.2	5.69	3.8	3.5
-2.0	9.52	-2.40	9.52	11.92	42	151.2	8.95	5.9	5.5
-1.0	10.51	-1.40	10.51	11.91	41	147.6	11.25	7.6	7.1
0.0	11.48	-0.40	11.48	11.88	41	147.6	14.06	9.5	8.9
1.0	12.44	0.60	12.44	11.84	41	147.6	17.54	11.9	11.1
2.0	13.37	1.60	13.37	11.77	41	147.6	21.73	14.7	13.7
3.0	14.26	2.60	14.26	11.66	40	144.0	26.67	18.5	17.3
4.0	14.98	3.60	14.98	11.38	40	144.0	31.48	21.9	20.3
5.0	15.37	4.60	15.37	10.77	40	144.0	34.43	23.9	21.9

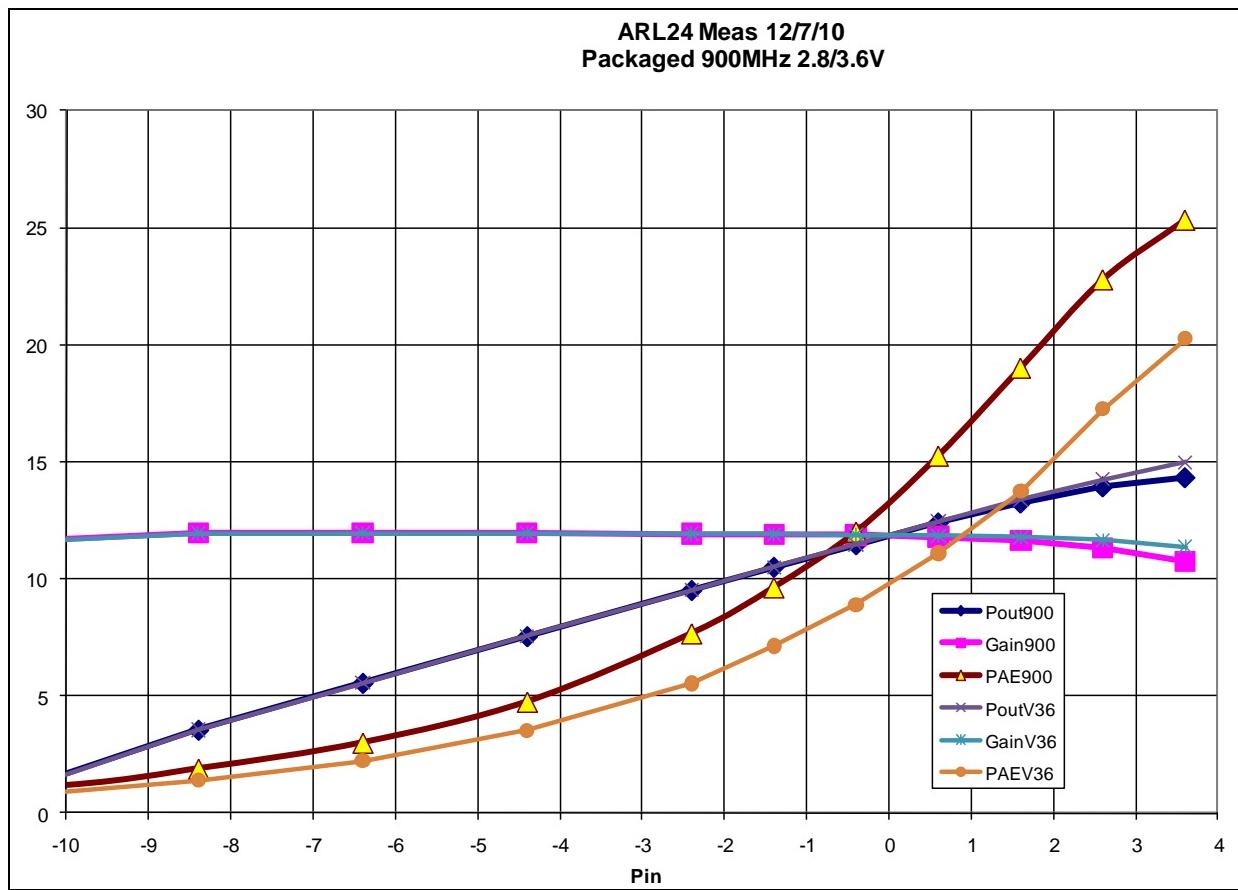


Figure 56. ARL24DB power performance at 900 MHz (2.8/3.6 V).

On the receive side, the noise figure and gain were measured at 450 MHz to be 15 dB and 3.6 dB, respectively, and 13.7 dB gain and 3.7 dB noise figure at 900 MHz. The gain was about as expected but the noise figure was slightly higher than that predicted by simulations.

4. Summary of Active Booster IC Designs

Several goals were targeted for an improved 2nd pass Booster IC. First, was re-tuning the designs to center around 425 MHz operation. Optimally, the supply voltage would be 2.8 V, but the designs should be robust over a range of supply voltages, with 3.6 V as a secondary target for optimal performance. Good output power (50–100 mW) and good efficiency (40–50% PAE) were desired, as was a low noise figure (less than 3 dB). The original TR switch was broadband but had more loss than was desired, so the redesigned 2nd pass TR switch was targeted for less than 0.5 dB insertion loss with positive voltage control and sufficient power handling capability to work with a 100 mW RF output power. Lastly, a broadband or dual band operation was desired. For these goals, the active designs were successful. The noise figure was a bit higher than the goal and the efficiency of the 50 mW design was good at the higher end of the band, but was less than desired at the 425 MHz center. Additional designs from the ARL 2nd pass TQPED GaAs tile integrated matching circuits for a COTS RFIC to improve size, weight, and power (SWAP) at the board level were intended to work with these active Booster IC designs, but will be tested separately in a wireless system.

Following is a tabular summary of the four active designs:

Design	Freq	GainT	Pout(mW)	PAE	GainR	NF	PDC(Tr)	PDC(Rc)
ARL21	425M	19.1/16.1	71/100	37/37	10.8	3.7	182/270	9/11
ARL22	425M	14.7/11.7	37/36	26/20	10.6	4.5	140/180	9/11
ARL23	425M	15.3/12.3	30/44	36/34	10.6	4.1	84/130	9/11
ARL24	425M	14.7/11.7	30/42	34/31	15.0	3.6	90/133	25/32
“ ”	900M	11.6/10.6	27/34	28/24	13.7	3.7	98/144	25/32

Notes: GainT is SS gain and compressed gain in dB, Pout is in mW at 2.8V/3.6V, PAE is % at 2.8V/3.6V, GainR is gain in dB of LNA, NF is in dB, P(Tr) is the transmit power consumption in mW at 2.8V/3.6V, and P(Re) is the power consumption in mW of the LNA at 2.8V/3.6V.

Following is a tabular summary of the test circuit (ARL25) amplifier designs:

Design	Freq	GainT	Pout(mW)	PAE	GainR	NF	PDC(Tr)	PDC(Rc)
PA 100m	425M	21.6/18.6	72/104	33/34	-	-	218/310	-
PA 50m	425M	18.5/15.5	43/50	29/25	-	-	148/202	-
LNA	425M	-	-	-	10.0	2.8	-	9/11

Note that the dual band design is not 3 dB compressed in the table, as the small signal gain was low and was not tested at higher compression levels. Overall, the 100 mW design (ARL21) seems to be closest to the goals set for the design. It would be desirable to improve the power added efficiency, but increasing the drive level for higher output powers with better efficiency reduces the gain. The dual band design, ARL24, was a compromise of performance in order to achieve a broadband operation. If broadband is desired, maybe this design can be further optimized for additional gain, output power, and efficiency.

5. Conclusions

Many thanks to those who helped with these designs, such as Khamsouk Kingkeo who wire bonded the designs in the QFN packages, and Russ Harris, who attached the QFN packages to the PC boards he designed for the 1st pass Booster IC tests, and soldered SMA connectors and DC supply bypass capacitors to these boards. See the references for documentation of the design, bare die tests, and packaged tests for the 1st and 2nd pass Booster IC designs. The passive designs will have to be tested at a system level and will be documented at a later date. The active designs show much promise for boosting the range and performance of wireless sensors, systems, and communications using COTS RFICs.

6. References

1. Mitchell, G.; Penn, J. *Preliminary Gallium Arsenide (GaAs) Integrated Circuit Design for Radio Frequency Booster Chips at 450, 900, and 2400 MHz*; ARL-TR-4970; U.S. Army Research Laboratory: Adelphi, MD, September 2009.
2. Penn, J. *GaAs Microwave Integrated Circuit Designs Submitted to TriQuint Semiconductor for Fabrication*; ARL-TN-0381; U.S. Army Research Laboratory: Adelphi, MD, December 2009.
3. Mitchell, G.; Penn, J. *Results of Bare Die Probing for RF Booster Chip at 400, 900, 2400 MHz*; ARL-TR-5170; U.S. Army Research Laboratory: Adelphi, MD, April 2010.
4. Penn, J. *Testing of GaAs Microwave Integrated Circuit Designs in QFN Packages*; ARL-TR-5131; U.S. Army Research Laboratory: Adelphi, MD, March 2010
5. Penn, J. *GaAs Microwave Integrated Circuit Designs Submitted to TriQuint Semiconductor for Fabrication (ARL Tile #2)*; ARL-TN-0404; U.S. Army Research Laboratory: Adelphi, MD, September 2010.
6. Penn, J. *Optimized (2nd Pass) Gallium Arsenide (GaAs) Integrated Circuit Radio Frequency (RF) Booster Designs for 425 MHz and Dual Band (425 and 900 MHz)*; ARL-TR-5396; U.S. Army Research Laboratory: Adelphi, MD, November 2010.
7. Penn, J. *Results of Bare Die Testing of Optimized (2nd Pass) Gallium Arsenide (GaAs) Integrated Circuit Radio Frequency (RF) Booster Designs for 425 MHz and Dual Band (425 and 900 MHz)*; ARL-TR-XXX; U.S. Army Research Laboratory: Adelphi, MD, January 2011.

List of Symbols, Abbreviations, and Acronyms

BPSK	binary phase shift keying
COTS	Commercial Off the Shelf
GaAs	gallium arsenide
IC	Integrated Circuit
MMIC	monolithic microwave integrated circuit
PAE	power added efficiency
PC	printed circuit
QFN	quad flat no lead
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
SWAP	size, weight, and power
TR	transmit/receive
UHF	ultra-high frequency

NO. OF COPIES	ORGANIZATION	<u>ABERDEEN PROVING GROUND</u>
1 (PDF only)	DEFENSE TECHNICAL INFORMATION CTR DTIC OCA 8725 JOHN J KINGMAN RD STE 0944 FORT BELVOIR VA 22060-6218	1 DIR USARL RDRL CIM G (BLDG 4600)
1	DIRECTOR US ARMY RESEARCH LAB IMNE ALC HRR 2800 POWDER MILL RD ADELPHI MD 20783-1197	
1	DIRECTOR US ARMY RESEARCH LAB RDRL CIM L 2800 POWDER MILL RD ADELPHI MD 20783-1197	
1	DIRECTOR US ARMY RESEARCH LAB RDRL CIM P 2800 POWDER MILL RD ADELPHI MD 20783-1197	
11	DIRECTOR US ARMY RESEARCH LAB RDRL SER PAUL AMIRTHARAJ RDRL SER E ROMEO DEL ROSARIO GREG MITCHELL JAMES WILSON GLEN BIRDWELL ROB REAMS JOHN PENN (3 HCS) ED VIVEIROS RDRL SEG STEVE RAGER 2800 POWDER MILL RD ADELPHI MD 20783-1197	
1	CERDEC I2WD RDER IWR CI BOB GROSS SUITE D 6240 GUARDIAN GATEWAY APG MD 21005	
1	I2WD STEVE HAUGHT FT MONMOUTH NJ	

INTENTIONALLY LEFT BLANK.